EPIC-QM77

EPIC Board

User's Manual 4th Ed

Last Updated: March 10, 2016

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● EPIC-QM77	1
● 1702150155 SATA power cable	1
● 1709070500 SATA cable	1
● M10QM77000 heat spreader	1
● 9657666600 jumper cap	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	EPIC Board
Processor	Intel® Core™ i7/i5/i3/Celeron® Processor
System Memory	204-pin SODIMM DDR3/L 1333/1600MHz Memory up to 8 GB
Chipset	Intel® QM77/HM76
I/O Chipset	Fintek 81866D
Ethernet	Intel 82579LM x 1/Intel 82583V x 1 10/100/1000Base LANs, RJ-45 x 2 Intel 82583V shared with Intel 82574L (Supports IEEE1588)
BIOS	AMI BIOS 64Mbit SPI ROM
Wake On LAN	Yes
Watchdog Timer	Generates a time-out system reset
H/W Status Monitoring	Supports power supply voltages, fan speed, and temperature monitoring
Expansion Interface	PCI/104 x 1
Battery	+12 V
Power Consumption (Typical)	38 W
Board Size	165 x 115 mm (6.5 x 4.53")
Gross Weight	0.4 kg (0.88 lbs)

- **Operating Temperature** 0 ~ 60°C (32 ~ 140°F)
- **Storage Temperature** -40 ~ 70°C (-40 ~ 158°F)
- **Operation Humidity** 10 ~ 80%, non-condensing

Display

- **Chipset** Processor-integrated
- **Memory** Shared system memory up to 512 MB
- **Resolution** CRT up to 1920 x 1200 @ 60Hz
  LCD up to 1920 x 1200 @ 60Hz
  Display Port up to 3840 x 2160 @ 60Hz
- **Display Combination** CRT/LCV simultaneous/ dual view
- **LCD Interface** VGA, LVDS1, DP, LVDS2 (Optional), eDP (Optional)

I/O

- **USB** USB 3.0 x 2
  USB 2.0 x 4 (with box header)
- **Serial Port** RS-232 x 5
  RS-232/422/485 x 1 (COM2)
- **Parallel Port** SPP/EPP/ECP Mode
- **DI/O** 16-bit (programmable)
- **Audio** Line-in
  Line-out
  Mic-in

CN-in

- **Keyboard/ Mouse** PS/2 Keyboard & Mouse x 1

*Note on OS

For Linux, AAEON suggests the following:

- Kernel 2.6.39 version or later: Set default BIOS/SATA operating mode to **IDE**

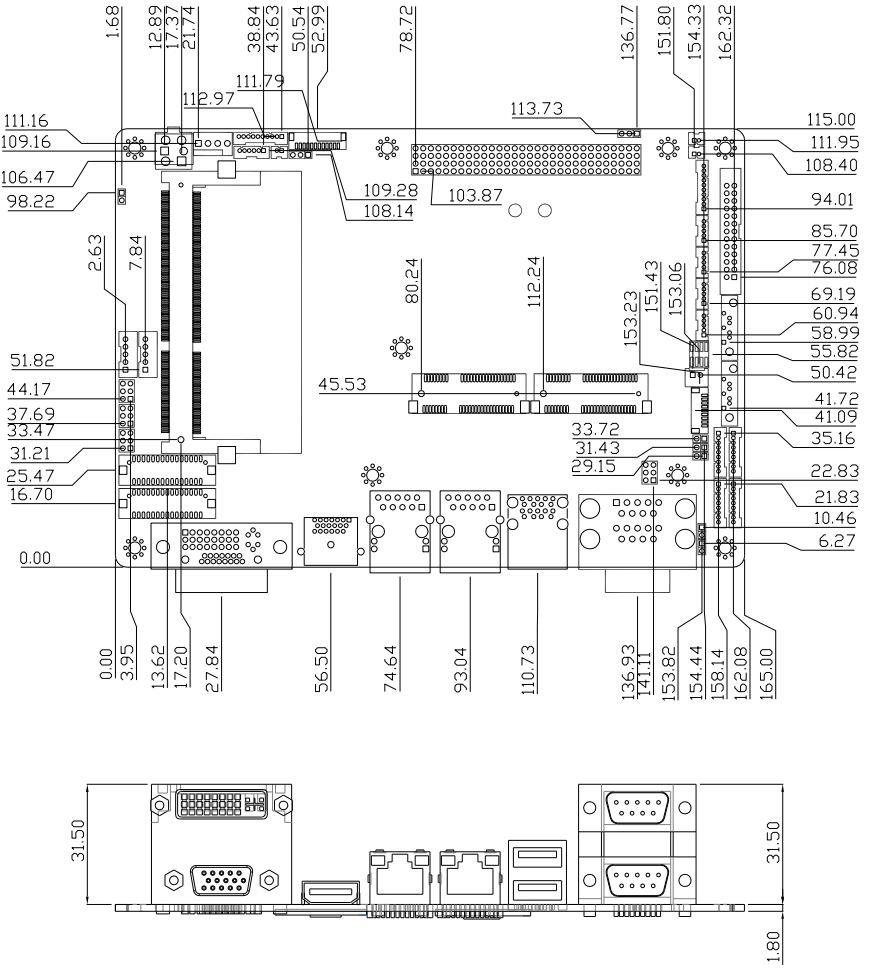
- Use Ubuntu 12.04 version or later for better display performance

Chapter 2

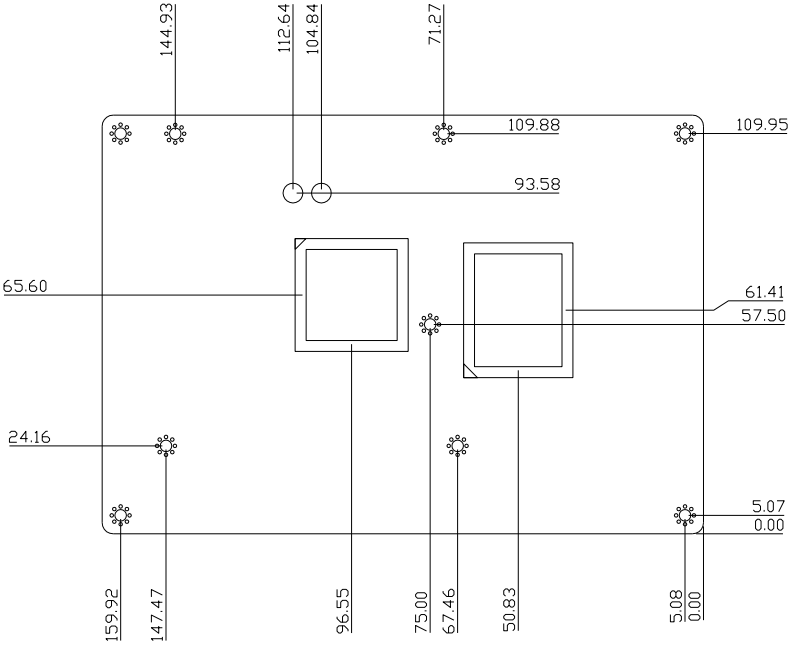
Hardware Information

2.1 Dimensions

Component Side



Solder Side


144.93
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109.95
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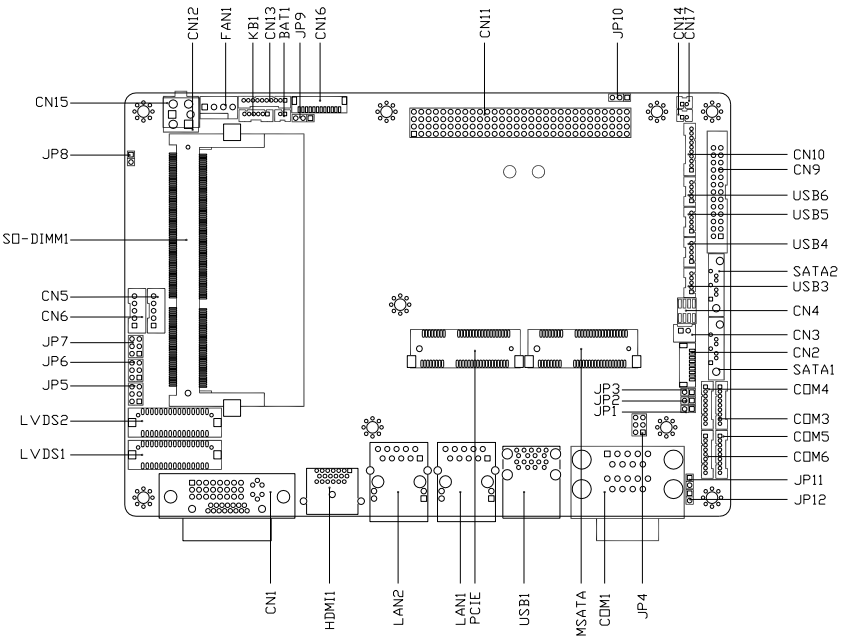
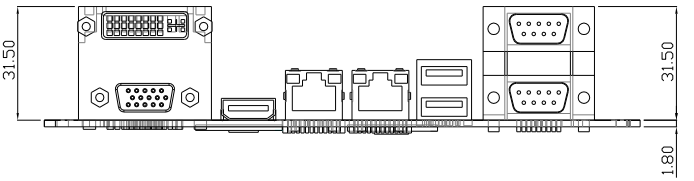
65.60
61.41
57.50
24.16
5.07
0.00
159.92
147.47
96.55
75.00
67.46
50.83
5.08
0.00

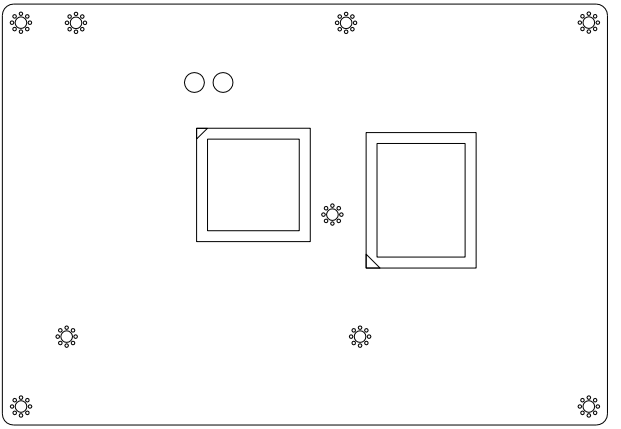
2.2 Jumpers and Connectors

Component Side





Solder Side

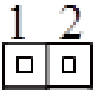


2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	LPT_DIO Selection
JP2	AT/ATX Selection
JP3	Touch Screen Connector Selection
JP4	Ring/12V/5V Selection
JP5	LCD VCC Selection
JP6	LCD Backlight Voltage Selection
JP7	LCD Backlight Control Selection
JP8	DDR3/DDR3L Voltage Selection
JP9	Clear CMOS
JP10	VIO104 Power Selection
JP11	mSATA/ PCIe Selection
JP12	COM2 Slew Selection

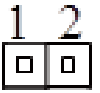
2.3.1 LPD/DIO Selection (JP1)



LPT

DI/O

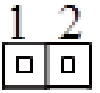
2.3.2 AT/ATX Selection (JP2)



ATX

AT

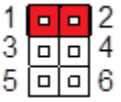
2.3.3 Touchscreen Selection (JP3)



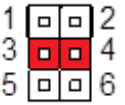
5-wire

4,8-wire

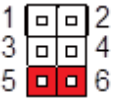
2.3.4 Touchscreen 4/5/8 Wire Mode Selection (JP4)



+12 V

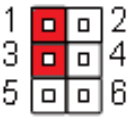
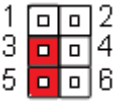


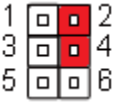
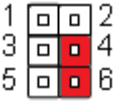
RI2#_SEL



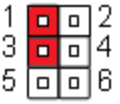
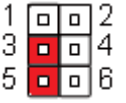
+5 V

2.3.5 LCD VCC Selection (JP5)

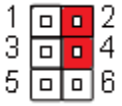
LVDS 1	
	
LVDS1 +5V (Default)	LVDS1 +3.3V

LVDS 2	
	
LVDS2 +5V (Default)	LVDS2 +3.3V

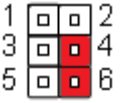
2.3.6 LCD Backlight Voltage Selection (JP6)

LVDS 1	
	
LVDS1 +5V (Default)	LVDS1 12V

LVDS 2



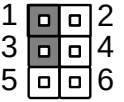
LVDS2 +5V (Default)



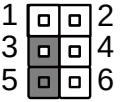
LVDS2 12V

2.3.7 LCD Backlight Control Selection (JP7)

LVDS 1

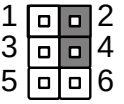


LVDS1 Voltage mode

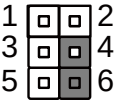


LVDS1 PWM mode

LVDS 2

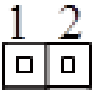


LVDS2 Voltage mode

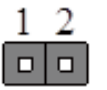


LVDS2 PWM mode

2.3.8 DDR /DDRL Selection (JP8)

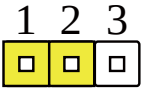


DDR3

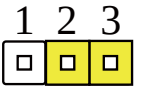


DDR3L

2.3.9 Clear CMOS Selection (JP9)

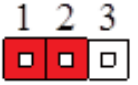


Normal



Clear CMOS

2.3.10 PCI-104 I/O Voltage Selection (JP10)



+5 V

+3.3 V

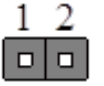
2.3.11 mSATA/PCIe Selection (JP11)

mSATA

PCIe

2.3.12 COM2 Slew Selection (JP12)

250k



1M/10M

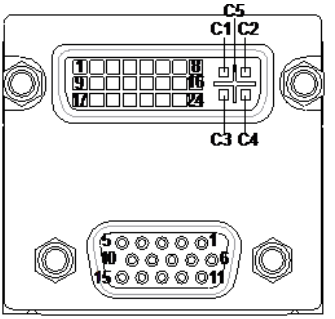
2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	VGA / DVI Dual Connector
CN2	Touch Screen Connector
CN3	SATA Power Connector
CN4	SPI Flash Header
CN5	1st Backlight Connector
CN6	2nd Backlight Connector
CN7	1st Mini Card Slot
CN8	2nd Mini Card Slot
CN9	LPT_DIO Connector
CN10	Audio Connector
CN11	PCI-104 Slot
CN12	4-Pin Power In Connector
CN13	Front Panel Connector
CN14	Amp R-channel Connector
CN15	2-Pin Power in Connector
CN16	LPC Connector
CN17	Amp L-channel Connector
CN18	3G SIM Connector
LAN1	1000 Base-TX Ethernet Connector
LAN2	1000 Base-TX Ethernet Connector
USB1	Dual USB3.0 Connector
USB3	USB2.0 Connector
USB4	USB2.0 Connector

USB5	USB2.0 Connector
USB6	USB2.0 Connector
COM1(Dual A)	COM1 RS-232 Serial Port Connector
COM1(Dual B)	COM2 RS-232/422/485 Serial Port Connector
COM3	COM3 RS-232 Serial Port Connector
COM4	COM4 RS-232 Serial Port Connector
COM5	COM5 RS-232 Serial Port Connector
COM6	COM6 RS-232 Serial Port Connector
SATA1	SATA Connector
SATA2	SATA Connector
KB1	PS/2 Keyboard Mouse Connector
FAN1	Fan Connector
HDMI1	HDMI Connector
BAT1	RTC Battery Connector
LVDS1	1st LVDS Connector
LVDS2	2nd LVDS Connector

2.4.1 VGA & DVI-I Connector (CN1)



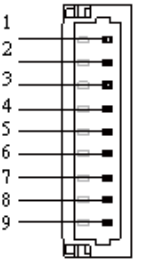
VGA			
Pin	Pin Name	Signal Type	Signal Level
1	RED	I/O	
2	GREEN	I/O	
3	BLUE	I/O	
4	NC		
5	GND	GND	
6	GND	GND	
7	GND	GND	
8	GND	GND	
9	V5S_DISP	PWR	5V
10	CRT_PLUG#	IN	
11	NC		
12	DDC_DATA	I/O	
13	HSYNC	I/O	
14	VSYNC	I/O	
15	DDC_CLK	I/O	

DVI			
Pin	Pin Name	Signal Type	Signal Level

1	DVI_DATA2_N	I/O	
2	DVI_DATA2_P	I/O	
3	GND	GND	
4	NC		
5	NC		
6	DVI_SCL	I/O	
7	DVI_SDA	I/O	
8	VSYNC	I/O	
9	DVI_DATA1_N	I/O	
10	DVI_DATA1_P	I/O	
11	GND	GND	
12	NC		
13	NC		
14	V5S_DISP	PWR	5V
15	D_CRT_PLUG#	IN	
16	DVI_HPD	I/O	
17	DVI_DATA0_N	I/O	
18	DVI_DATA0_P	I/O	
19	GND	GND	
20	NC		
21	NC		
22	GND	GND	
23	DVI_CLK_P	I/O	
24	DVI_CLK_N	I/O	
C1	RED	I/O	
C2	GREEN	I/O	
C3	BLUE	I/O	
C4	HSYNC	I/O	
C5	GND	GND	

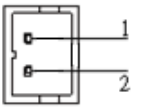
C6	GND	GND

2.4.2 Touch Screen Connector (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	Y-	IN	
3	Y+	IN	
4	X-	IN	
5	X+	IN	
6	SENSE	IN	
7	Y+	IN	
8	X-	IN	
9	X+	IN	

2.4.3 SATA Power Connector (CN3)

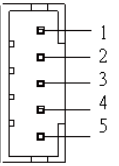


Pin	Pin Name	Signal Type	Signal Level
1	V5S	PWR	+5V
2	GND	GND	GND

2.4.4 SPI Flash Header (CN4)

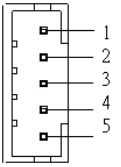
Pin	Pin Name	Signal Type	Signal Level
1	V3.3M_SPI	PWR	+3.3V
2	GND	GND	
3	SPI_CE#_F	IN	
4	SPI_CLK_F	I/O	
5	SPI_SO_F	OUT	
6	SPI_SI_F	IN	
7			
8			

2.4.5 1st Backlight Connector (CN5)



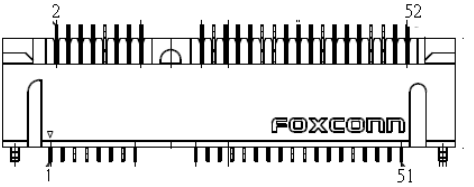
Pin	Pin Name	Signal Type	Signal Level
1	VCC_LVDS_BKLT1	PWR	+5V OR +12V
2	L_BRIGHTNESS1	OUT	
3	GND	GND	
4	GND	GND	
5	BKLT_EN1	OUT	

2.4.6 2nd Backlight Connector (CN6)



Pin	Pin Name	Signal Type	Signal Level
1	VCC_LVDS_BKLT2	PWR	+5V OR +12V
2	L_BRIGHTNESS2	OUT	
3	GND	GND	
4	GND	GND	
5	BKLT_EN2	OUT	

2.4.7 1st MiniCard Slot (CN7)

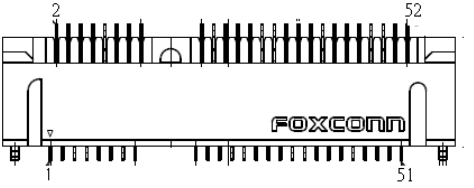


Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	OUT	
2	V3.3_MINICARD1	PWR	+3.3V
3	Reserved		
4	GND	GND	
5	Reserved		
6	+V1.5S	PWR	+1.5V
7	CLK_PCIE_REQ#_MPCIE	OUT	
8	Reserved		
9	GND	GND	

10	Reserved		
11	CLK_PCIE_MPCIE_N	I/O	
12	Reserved		
13	CLK_PCIE_MPCIE_P	I/O	
14	Reserved		
15	GND	GND	
16	Reserved		
17	Reserved		
18	Reserved		
19	Reserved		
20	MINI_DISABLE#	IN	
21	XSD	OUT	
22	BUF_PLT_RST#	IN	
23	PERn0_RX+	I/O	
24	+V3.3_MINICARD1	PWR	+3.3V
25	PERp0_RX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+V1.5S	PWR	+1.5V
29	GND	GND	
30	SMB_CLK_SBY	I/O	
31	PETn0_TX-	I/O	
32	SMB_DATA_SBY	I/O	
33	PETp0_TX+	I/O	
34	GND	GND	
35	GND	GND	
36	USB_PN2	I/O	
37	GND	GND	
38	USB_PP2	I/O	

39	+V3.3_MINICARD1	PWR	+3.3V
40	GND	GND	
41	+V3.3_MINICARD1	PWR	+3.3V
42	Reserved		
43	NC		
44	Reserved		
45	Reserved	I/O	
46	Reserved		
47	Reserved	I/O	
48	+V1.5S	PWR	+1.5V
49	Reserved	I/O	
50	GND	GND	
51	Reserved	I/O	
52	+V3.3_MINICARD1	PWR	+3.3V

2.4.8 2nd MiniCard Slot (CN8)

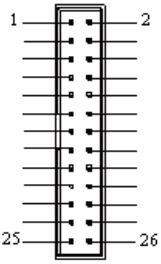


Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	OUT	
2	+V3.3_MINICARD2	PWR	+3.3V
3	Reserved		
4	GND	GND	
5	Reserved		
6	+V1.5S	PWR	+1.5V

7	CLK_PCIE_REQ#_MINI2	OUT	
8	Reserved		
9	GND	GND	
10	Reserved		
11	CLK_PCIE_MINI2_N	I/O	
12	Reserved		
13	CLK_PCIE_MINI2_P	I/O	
14	Reserved		
15	GND	GND	
16	Reserved		
17	Reserved		
18	Reserved		
19	Reserved		
20	MINI_DISABLE#	IN	
21	GND	GND	
22	BUF_PLT_RST#	IN	
23	PCIE_RXN6	I/O	
24	+V3.3_MINICARD2	PWR	+3.3V
25	PCIE_RXP6	I/O	
26	GND	GND	
27	GND	GND	
28	+V1.5S	PWR	+1.5V
29	GND	GND	
30	SMB_CLK_SBY	I/O	
31	PCIE_TNX6	I/O	
32	SMB_DATA_SBY	I/O	
33	PCIE_TXP6	I/O	
34	GND	GND	
35	GND	GND	

36	USB_PN7	I/O	
37	GND	GND	
38	USB_PP7	I/O	
39	+V3.3_MINICARD2	PWR	+3.3V
40	GND	GND	
41	+V3.3_MINICARD2	PWR	+3.3V
42	Reserved		
43	Reserved		
44	Reserved		
45	Reserved		
46	Reserved		
47	CL_CLK	I/O	
48	+V1.5S	PWR	+1.5V
49	CL_DATA	I/O	
50	GND	GND	
51	CL_RST#	IN	
52	+V3.3_MINICARD2	PWR	+3.3V

2.4.9 LPT Port Connector (CN9)



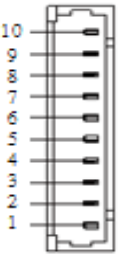
LPT Mode			
Pin	Pin Name	Signal Type	Signal Level
1	STOBE#	I/O	

2	#AFD	I/O
3	PPD0	I/O
4	ERR#	I/O
5	PPD1	I/O
6	PINIT#	I/O
7	PPD2	I/O
8	SLIN#	I/O
9	PPD3	I/O
10	GND	GND
11	PPD4	I/O
12	GND	GND
13	PPD5	I/O
14	GND	GND
15	PPD6	I/O
16	GND	GND
17	PPD7	I/O
18	GND	GND
19	ACK#	I/O
20	GND	GND
21	BUSY	I/O
22	GND	GND
23	PE	I/O
24	GND	GND
25	SLCT	I/O
26	N.C	

DIO Mode			
Pin	Pin Name	Signal Type	Signal Level
1	GPIO7	I/O	

2	GPIO6	I/O
3	GPIO8	I/O
4	GPIO5	I/O
5	GPIO9	I/O
6	GPIO4	I/O
7	GPIO10	I/O
8	GPIO3	I/O
9	GPIO11	I/O
10	GND	GND
11	GPIO12	I/O
12	GND	GND
13	GPIO13	I/O
14	GND	GND
15	GPIO14	I/O
16	GND	GND
17	GPIO15	I/O
18	GND	GND
19	GPIO2	I/O
20	GND	GND
21	GPIO1	I/O
22	GND	GND
23	GPIO0	I/O
24	GND	GND
25	N.C	
26	N.C	

2.4.10 Audio Connector (CN10)

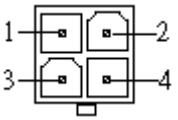


Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LIN_L	IN	
5	LIN_R	IN	
6	GND_AUDIO	GND	
7	LOUT_L	OUT	
8	GND_AUDIO	GND	
9	LOUT_R	OUT	
10	+5V_AUDIO	PWR	+5V

2.4.11 PCI/104 Connector (CN11)

	A	B	C	D
1	GND	+5V_SB	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	PSON#	PAR
10	GND	PERR#	+3.3V	PME#
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

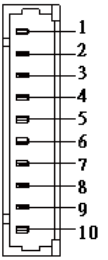
2.4.12 ATX 4Pin Power Connector (CN12)



Pin	Pin Name	Signal Type	Signal Level

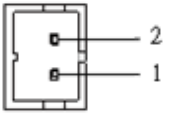
1	GND	GND	
2	GND	GND	
3	+12VSB	PWR	+12V
4	+12VSB	PWR	+12V

2.4.13 Front Panel Connector (CN13)



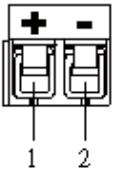
Pin	Pin Name	Signal Type	Signal Level
1	PWRSIN#	IN	
2	GND	GND	
3	+V5S	PWR	+5V
4	FP_SPKR#	IN	
5	+V3.3S	PWR	+3.3V
6	FP_HDLED#	IN	
7	+V3.3S	PWR	+3.3V
8	GND	GND	
9	HWRST#	IN	
10	GND	GND	

2.4.14 AMP-R Channel Connector (CN14)



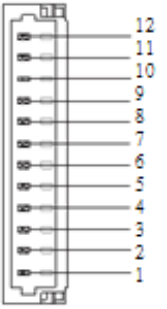
Pin	Pin Name	Signal Type	Signal Level
1	SPK_R+	OUT	
2	SPK_R-	OUT	

2.4.15 2-Pin Power Connector (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	+12VSB	PWR	+12V
2	GND	GND	

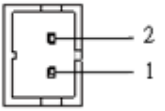
2.4.16 LPC Connector (CN16)



Pin	Pin Name	Signal Type	Signal Level
1	LPC_AD0	I/O	
2	LPC_AD1	I/O	
3	LPC_AD2	I/O	
4	LPC_AD3	I/O	
5	+V3.3S	PWR	+3.3V
6	LPC_FRAME#	IN	

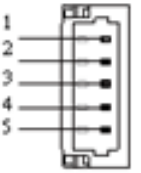
7	BUF_PLT_RST#	IN
8	GND	GND
9	CLK_LPC_33M	OUT
10	LPC_DRQ#0	OUT
11	LPC_DRQ#1	OUT
12	INT_SERIRQ	I/O

2.4.17 AMP-L Channel Connector (CN17)



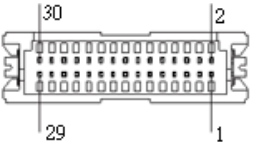
Pin	Pin Name	Signal Type	Signal Level
1	SPK_L+	OUT	
2	SPK_L-	OUT	

2.4.18 3G SIM Connector (CN18)



Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	+3.3V
2	UIM_DAT	I/O	
3	UIM_CLK	OUT	
4	UIM_RST	OUT	
5	UIM_VPP	GND	

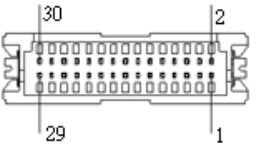
2.4.19 1st LVDS Connector (LVDS1)



Pin	Pin Name	Signal Type	Signal Level
1	BKLT_EN1	OUT	
2	L_BRIGHTNESS1	OUT	
3	+VDD_LVDS1	PWR	+3.3V OR +5V
4	GND	GND	
5	LVDSA_CLK#	OUT	
6	LVDSA_CLK	OUT	
7	+VDD_LVDS1	PWR	+3.3V OR +5V
8	GND	GND	
9	LVDSA_DATA0#	I/O	
10	LVDSA_DATA0	I/O	
11	LVDSA_DATA1#	I/O	
12	LVDSA_DATA1	I/O	
13	LVDSA_DATA2#	I/O	
14	LVDSA_DATA2	I/O	
15	LVDSA_DATA3#	I/O	
16	LVDSA_DATA3	I/O	
17	LVDS_DDC_DATA	I/O	
18	LVDS_DDC_CLK	I/O	
19	LVDSB_DATA0#	I/O	
20	LVDSB_DATA0	I/O	
21	LVDSB_DATA1#	I/O	
22	LVDSB_DATA1	I/O	

23	LVDSB_DATA2#	I/O	
24	LVDS_DATA2	I/O	
25	LVDSB_DATA3#	I/O	
26	LVDSB_DATA3	I/O	
27	+VDD_LVDS1	PWR	+3.3V OR +5V
28	GND	GND	
29	LVDSB_CLK#	I/O	
30	LVDSB_CLK	I/O	

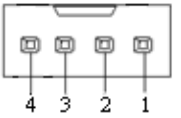
2.4.20 2nd LVDS Connector (LVDS2)



Pin	Pin Name	Signal Type	Signal Level
1	BKLT_EN2	OUT	
2	L_BRIGHTNESS2	OUT	
3	+VDD_LVDS2	PWR	+3.3V OR +5V
4	GND	GND	
5	LVDSC_CLK#	I/O	
6	LVDSC_CLK	I/O	
7	+VDD_LVDS2	PWR	+3.3V OR +5V
8	GND	GND	
9	LVDSC_DATA0#	I/O	
10	LVDSC_DATA0	I/O	
11	LVDSC_DATA1#	I/O	
12	LVDSC_DATA1	I/O	
13	LVDSC_DATA2#	I/O	

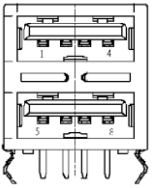
14	LVDSC_DATA2	I/O	
15	LVDSC_DATA3#	I/O	
16	LVDSC_DATA3	I/O	
17	LVDS_DDC_DATA_3460	I/O	
18	LVDS_DDC_CLK_3460	I/O	
19	LVDSD_DATA0#	I/O	
20	LVDSD_DATA0	I/O	
21	LVDSD_DATA1#	I/O	
22	LVDSD_DATA1	I/O	
23	LVDSD_DATA2#	I/O	
24	LVDSD_DATA2	I/O	
25	LVDSD_DATA3#	I/O	
26	LVDSD_DATA3	I/O	
27	+VDD_LVDS2	PWR	+3.3V OR +5V
28	GND	GND	
29	LVDSD_CLK#	I/O	
30	LVDSD_CLK	I/O	

2.4.21 Fan Connector (FAN1)



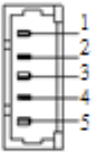
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_CTL	OUT	
3	FAN_TAC	OUT	
4	FAN_CTL_R	OUT	

2.4.22 USB3.0 Dual Connector (USB1)



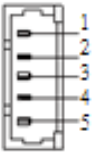
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_0	PWR	+5V
2	USBD0-	I/O	
3	USBD0+	I/O	
4	GND	GND	
5	USB3_RX0_CON_N	I/O	
6	USB3_RX0_COP_P	I/O	
7	GND	GND	
8	USB3_TX0_CON_N	I/O	
9	USB3_TX0_CON_P	I/O	
10	+V5A_USB_0	PWR	+5V
11	USBD1-	I/O	
12	USBD1+	I/O	
13	GND	GND	
14	USB3_RX1_CON_N	I/O	
15	USB3_RX1_CON_P	I/O	
16	GND	GND	
17	USB3_TX1_CON_N	I/O	
18	USB3_TX1_CON_P	I/O	

2.4.23 USB2.0 Connector (USB3)



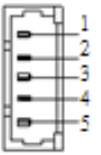
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_2	PWR	+5V
2	USBD9-	I/O	
3	USBD9+	I/O	
4	GND	GND	
5	GND	GND	

2.4.24 USB2.0 Connector (USB4)



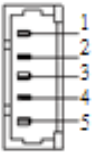
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_2	PWR	+5V
2	USBD12-	I/O	
3	USBD12+	I/O	
4	GND	GND	
5	GND	GND	

2.4.25 USB2.0 Connector (USB5)



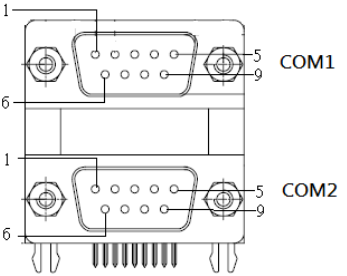
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_3	PWR	+5V
2	USBD10-	I/O	
3	USBD10+	I/O	
4	GND	GND	
5	GND	GND	

2.4.26 USB2.0 Connector (USB6)



Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_3	PWR	+5V
2	USBD13-	I/O	
3	USBD13+	I/O	
4	GND	GND	
5	GND	GND	

2.4.27 RS-232 Serial Port Dual Connector (COM1+COM2)



COM1 (RS-232)			
Pin	Pin Name	Signal Type	Signal Level
1	DCD#1	IN	
2	RXD#1	IN	
3	TXD1	OUT	
4	DTR#1	OUT	
5	GND	GND	
6	DSR#1	IN	
7	RTS#1	OUT	
8	CTS#1	IN	
9	RI#1	IN	

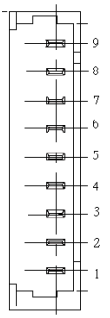
COM2 (RS-232)			
Pin	Pin Name	Signal Type	Signal Level
1	DCD#2	IN	
2	RXD#2	IN	
3	TXD2	OUT	
4	DTR#2	OUT	
5	GND	GND	
6	DSR#2	IN	

7	RTS#2	OUT	
8	CTS#2	IN	
9	RI#2/+5V/+12V	IN/PWR	

COM2 (RS-422)			
Pin	Pin Name	Signal Type	Signal Level
1	422TXD-	OUT	
2	422TXD+	OUT	
3	422RXD+	IN	
4	422RXD-	IN	
5	NC		
6	NC		
7	NC		
8	NC		
9	NC/+5V/+12V	PWR	+5V/+12V

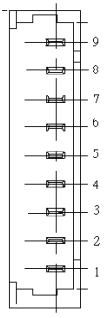
COM2 (RS-485)			
Pin	Pin Name	Signal Type	Signal Level
1	485D-	I/O	
2	485D+	I/O	
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	NC/+5V/+12V	PWR	+5V/+12V

2.4.28 RS-232 Serial Port Connector (COM4)



Pin	Pin Name	Signal Type	Signal Level
1	DCD#4	IN	
2	DSR#4	IN	
3	RXD4	IN	
4	RTS#4	OUT	
5	TXD4	OUT	
6	CTS#4	IN	
7	DTR#4	OUT	
8	RI#4	IN	
9	GND	GND	

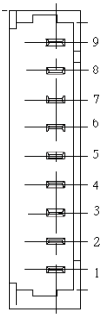
2.4.29 RS-232 Serial Port Connector (COM5)



Pin	Pin Name	Signal Type	Signal Level

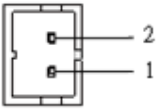
1	DCD#5	IN
2	DSR#5	IN
3	RXD5	IN
4	RTS#5	OUT
5	TXD5	OUT
6	CTS#5	IN
7	DTR#5	OUT
8	RI#5	IN
9	GND	GND

2.4.30 RS-232 Serial Port Connector (COM6)



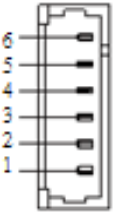
Pin	Pin Name	Signal Type	Signal Level
1	DCD#6	IN	
2	DSR#6	IN	
3	RXD6	IN	
4	RTS#6	OUT	
5	TXD6	OUT	
6	CTS#6	IN	
7	DTR#6	OUT	
8	RI#6	IN	
9	GND	GND	

2.4.31 Battery Connector (BAT1)



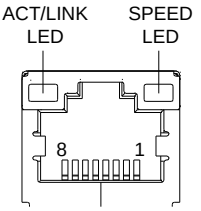
Pin	Pin Name	Signal Type	Signal Level
1	RTCBAT	PWR	+3.3V
2	GND	GND	

2.4.32 PS2 Keyboard and Mouse Connector (KB1)



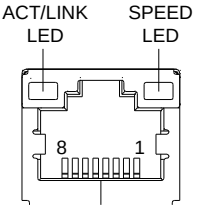
Pin	Pin Name	Signal Type	Signal Level
1	KBDATA	OUT	
2	KBCLK	OUT	
3	GND	GND	
4	+V5A_KBMS	PWR	+5V
5	MSDATA	OUT	
6	MSCLK	OUT	

2.4.33 LAN Ethernet RJ-45 Connector (LAN1)



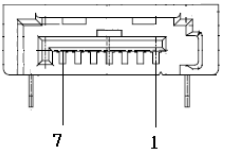
Pin	Pin Name	Signal Type	Signal Level
1	LAN1_MDIP0	I/O	
2	LAN1_MDIN0	I/O	
3	LAN1_MDIP1	I/O	
4	LAN1_MDIN1	I/O	
5	LAN1_MDIP2	I/O	
6	LAN1_MDIN2	I/O	
7	LAN1_MDIP3	I/O	
8	LAN1_MDIN3	I/O	

2.4.34 LAN Ethernet RJ-45 Connector (LAN2)



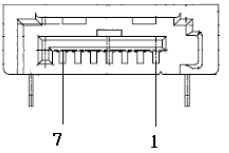
Pin	Pin Name	Signal Type	Signal Level
1	LAN2_MDIP0	I/O	
2	LAN2_MDIN0	I/O	
3	LAN2_MDIP1	I/O	
4	LAN2_MDIN1	I/O	
5	LAN2_MDIP2	I/O	
6	LAN2_MDIN2	I/O	
7	LAN2_MDIP3	I/O	
8	LAN2_MDIN3	DIFF.	
8	LAN1_MDIN3	I/O	

2.4.35 SATA Connector (SATA1)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TXP0	I/O	
3	SATA_TXN0	I/O	
4	GND	GND	
5	SATA_RXN0	I/O	
6	SATA_RXP0	I/O	
7	GND	GND	

2.4.36 SATA Connector (SATA2)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TXP1	I/O	
3	SATA_TXN1	I/O	
4	GND	GND	
5	SATA_RXN1	I/O	
6	SATA_RXP1	I/O	
7	GND	GND	

Chapter 3

BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

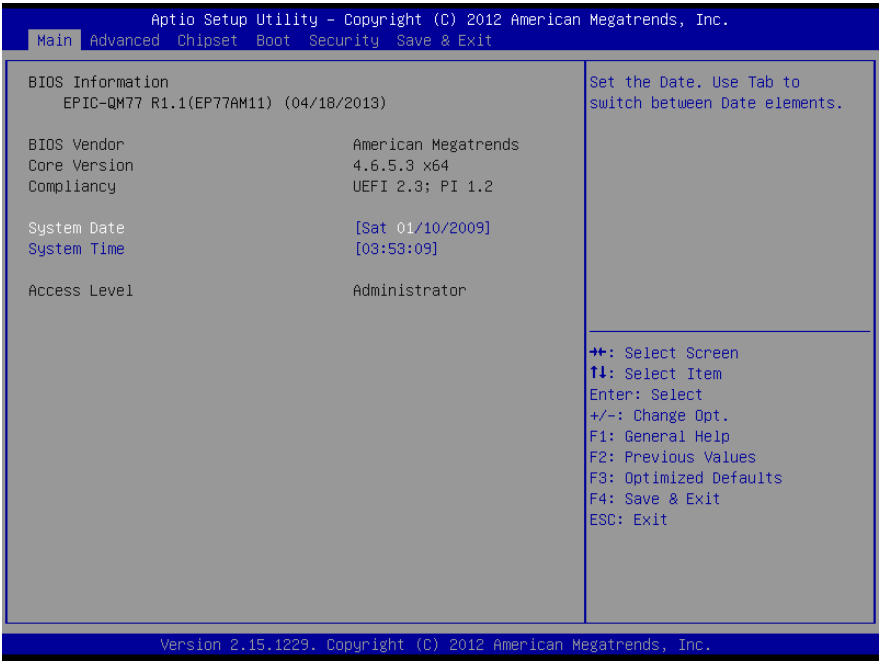
Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

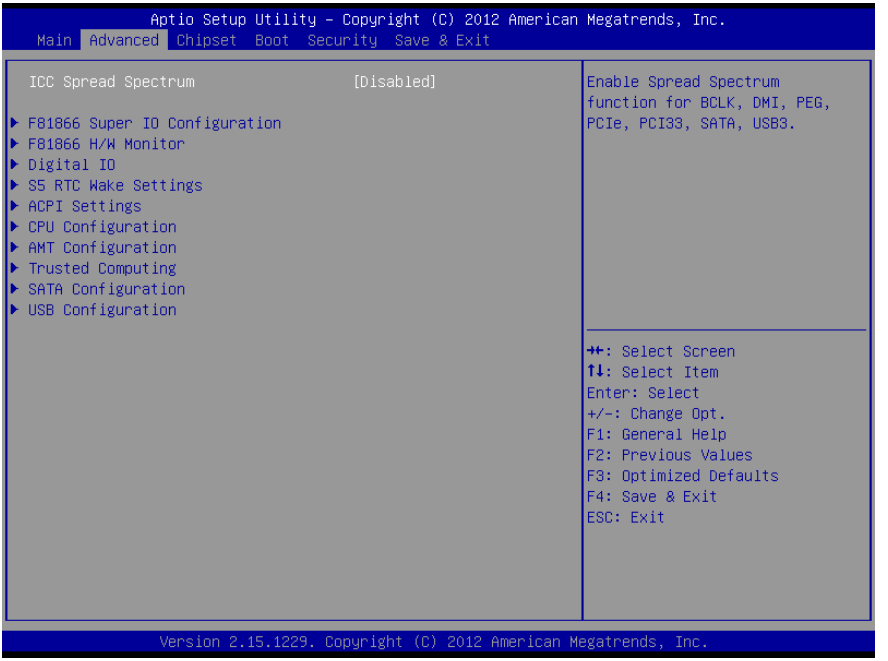
Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

3.3 Setup submenu: Main



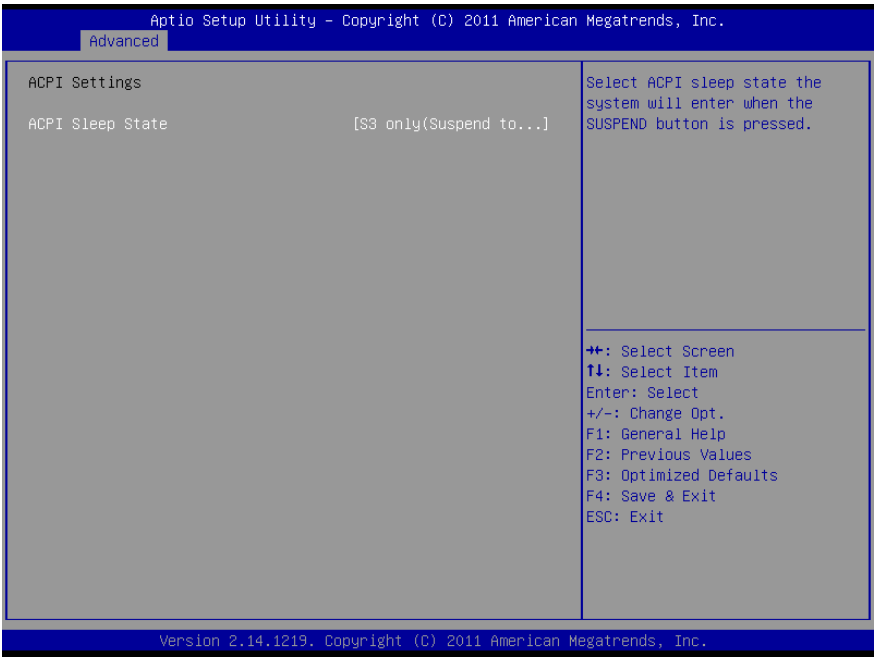
3.4 Setup submenu: Advanced



Options summary:

ICC Spread Spectrum	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Spread Spectrum function for BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3.		

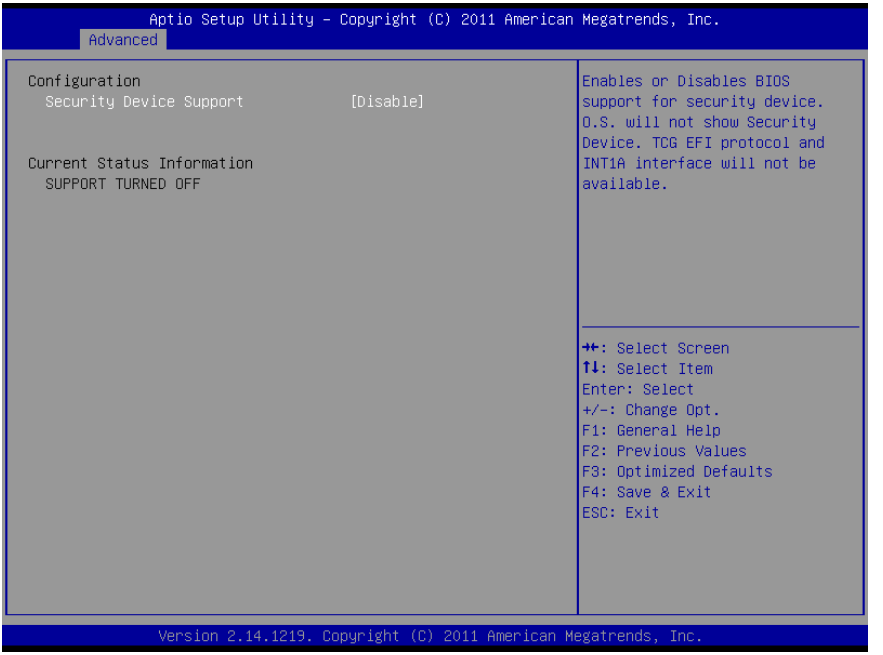
3.4.1 Advanced: ACPI Settings



Options summary:

Suspend mode	S1 only (CPU Stop Clock)	Optimal Default, Failsafe Default
	S3 only (Suspend to RAM)	
Select the ACPI state used for System Suspend		

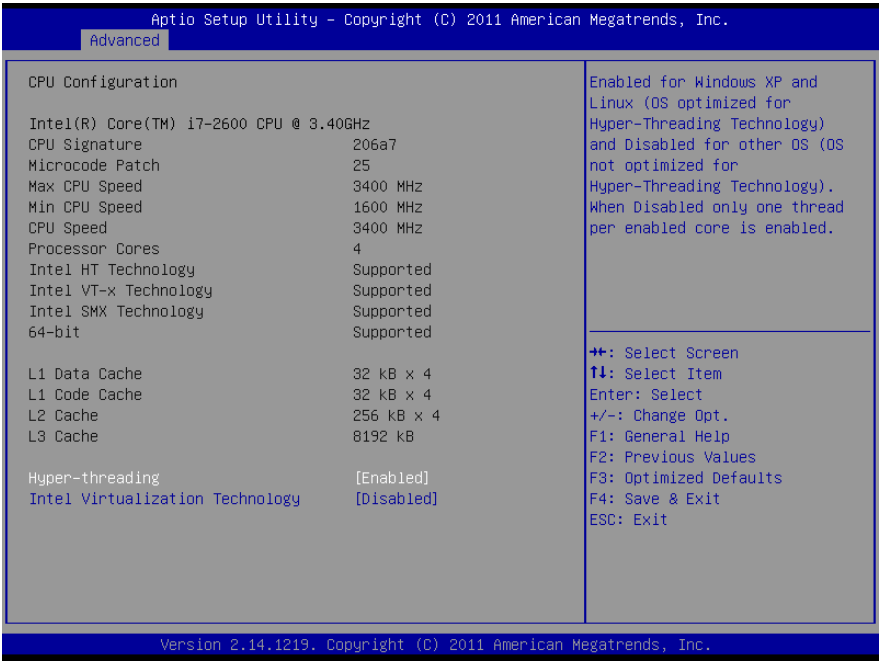
3.4.2 Advanced: Trusted Computing



Options summary:

Security Device Support	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		

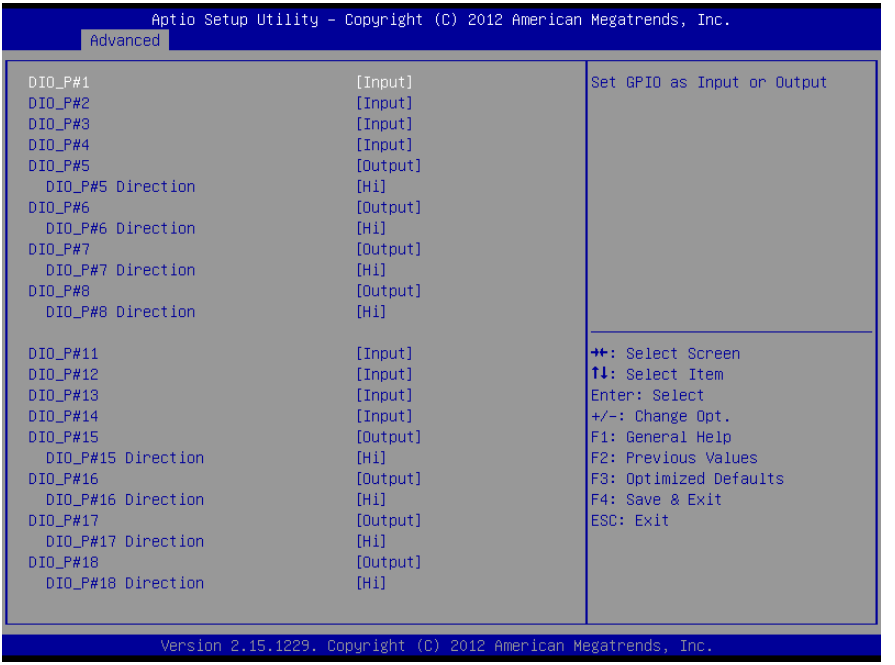
3.4.3 Advanced: CPU Configuration



Options summary:

Hyper-Threading	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable CPU Hyper-Threading function		
Intel Virtualization Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology		

3.4.4 Advanced: Digital IO

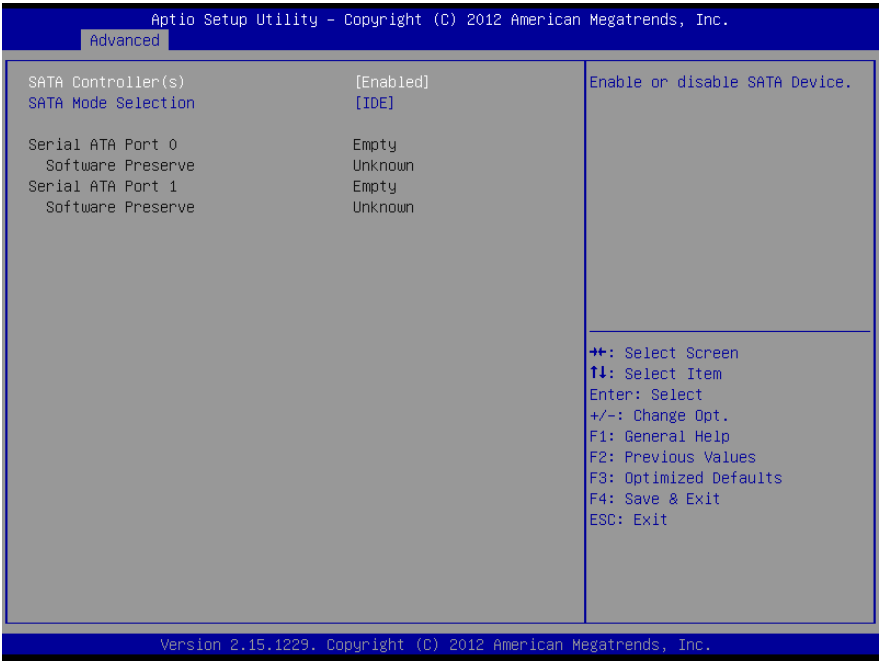


Options summary:

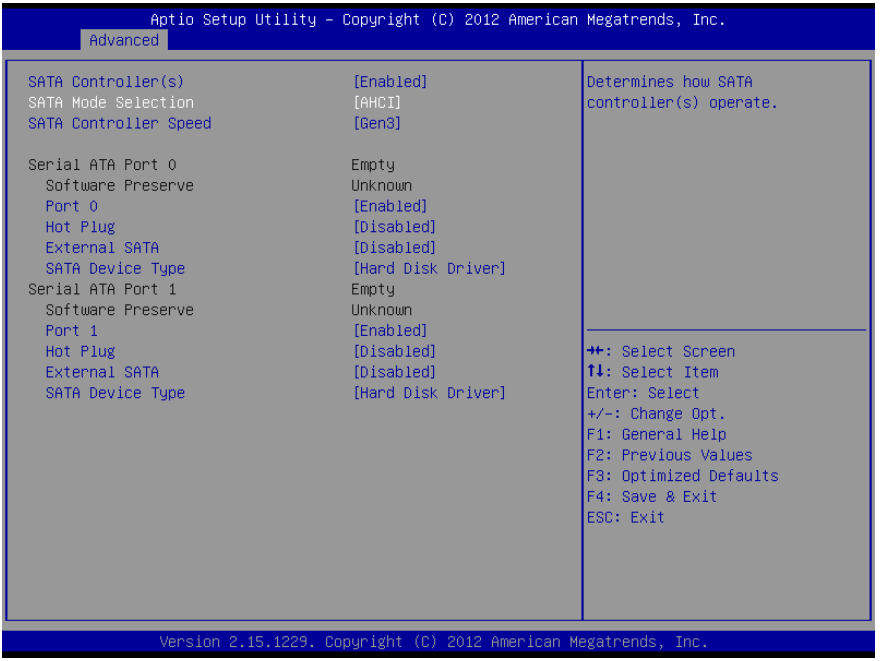
DIO_P#1~4	Input	Default
	Output	
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#5~8	Input	
	Output	Default
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#5~8 Direction	Low	
	Hi	Default
Allows BIOS to select high/low voltage level to output to corresponding DIO ping.		
DIO_P#11~14	Input	Default
	Output	
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#15~18	Input	
	Output	Default
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#15~18 Direction	Low	

	Hi	Default
Allows BIOS to select high/low voltage level to output to corresponding DIO ping.		

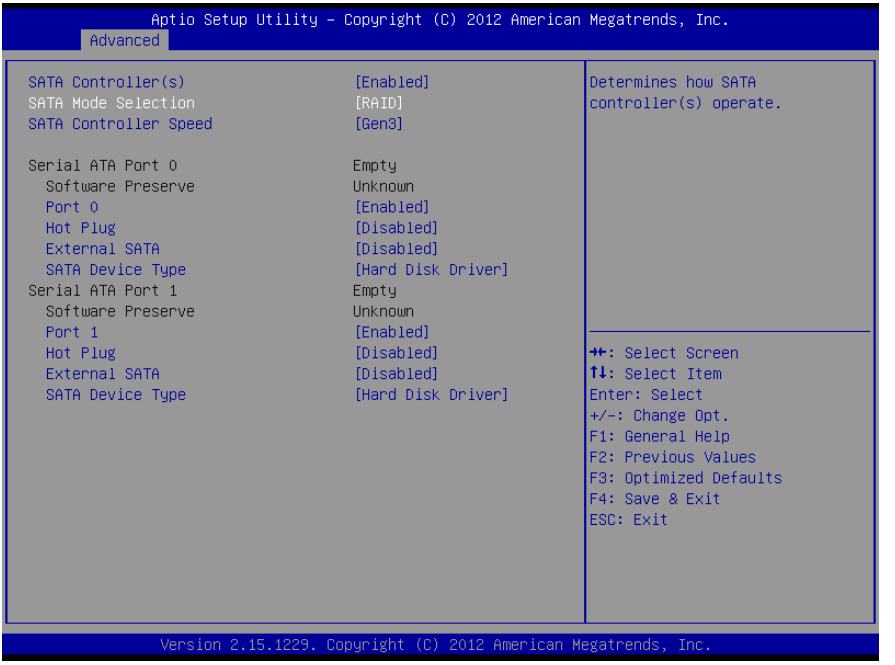
3.4.5 Advanced: IDE Configuration (IDE)



3.4.6 Advanced: IDE Configuration (AHCI)



3.4.7 Advanced: IDE Configuration (RAID)

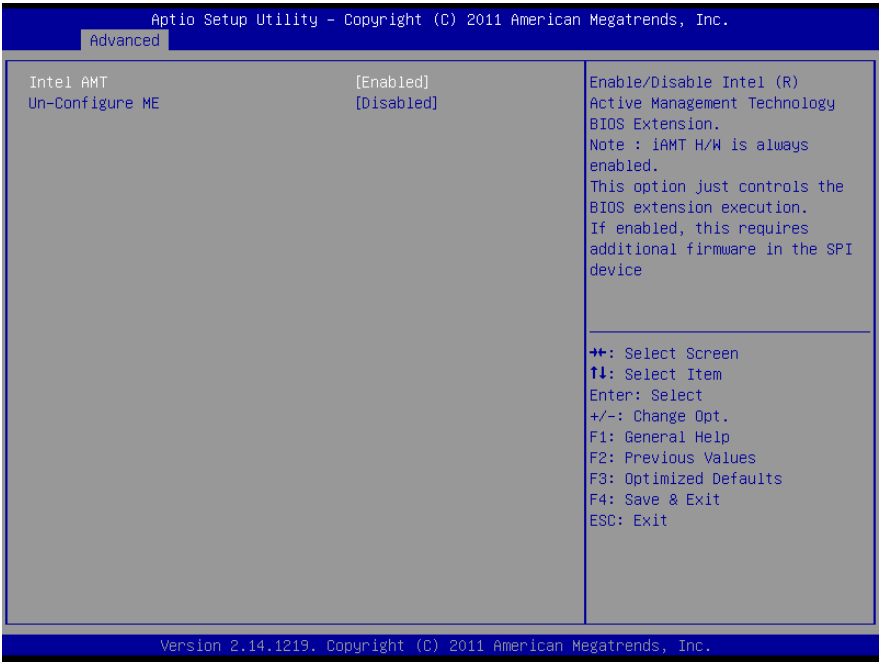


Options summary:

SATA Controllers	Disabled	
	Enabled	Default
En/Disable SATA Controller.		
SATA Mode	IDE	Default
	AHCI	
	RAID	
IDE: Configure SATA controllers as legacy IDEAHCI: Configure SATA controllers to operate in AHCI mode		
SATA Controller Speed	Gen1	
	Gen2	
	Gen3	Default
Indicates the maximum speed the SATA controller can support.		
Port x	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable SATA Port.		
Hot Plug	Disabled	

	Enabled	Optimal Default, Failsafe Default
En/Disable Hot Plug feature.		

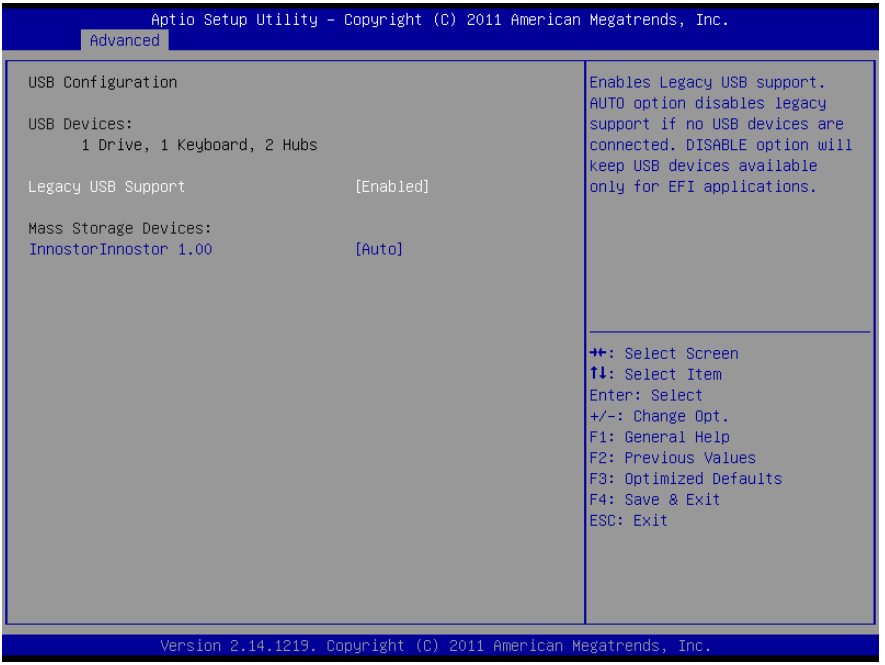
3.4.8 Advanced: AMT Configuration



Options summary:

Intel AMT	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Intel Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.		
Un-configure ME	Disabled	Optimal Default, Failsafe Default
	Enabled	
OEMFlag Bit 15: Un-Configure ME without password.		

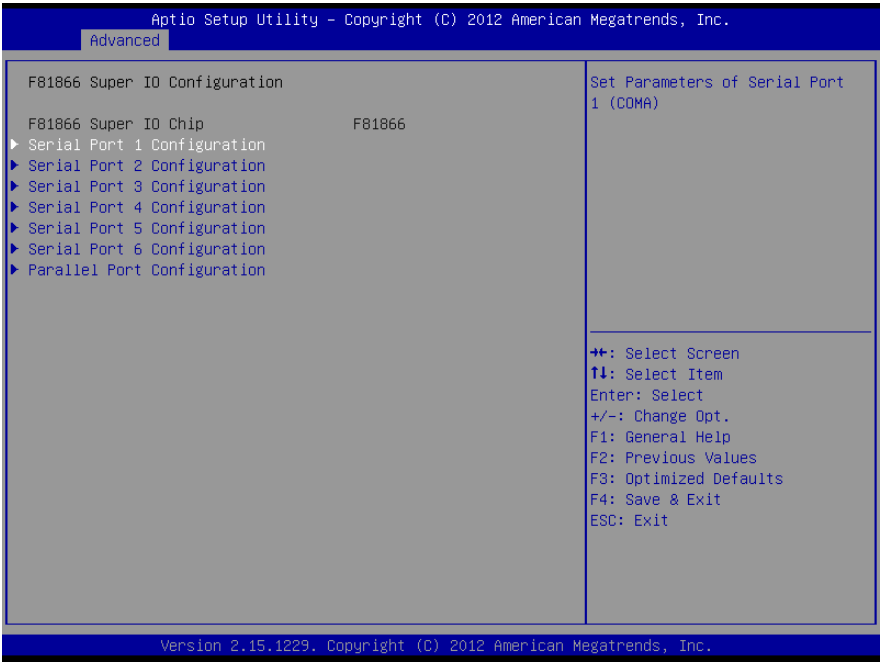
3.4.9 Advanced: USB Configuration



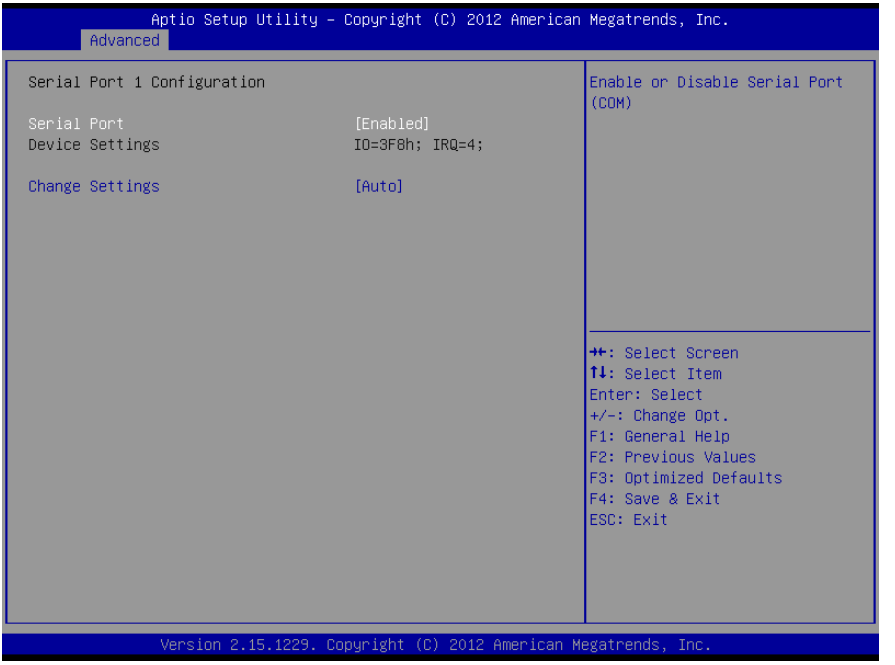
Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		
Device Name (Emulation Type)	Auto	Optimal Default, Failsafe Default
	Floppy	
	Forced FDD	
	Hard Disk	
	CDROM	
If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)		

3.4.10 Advanced: Super IO Configuration



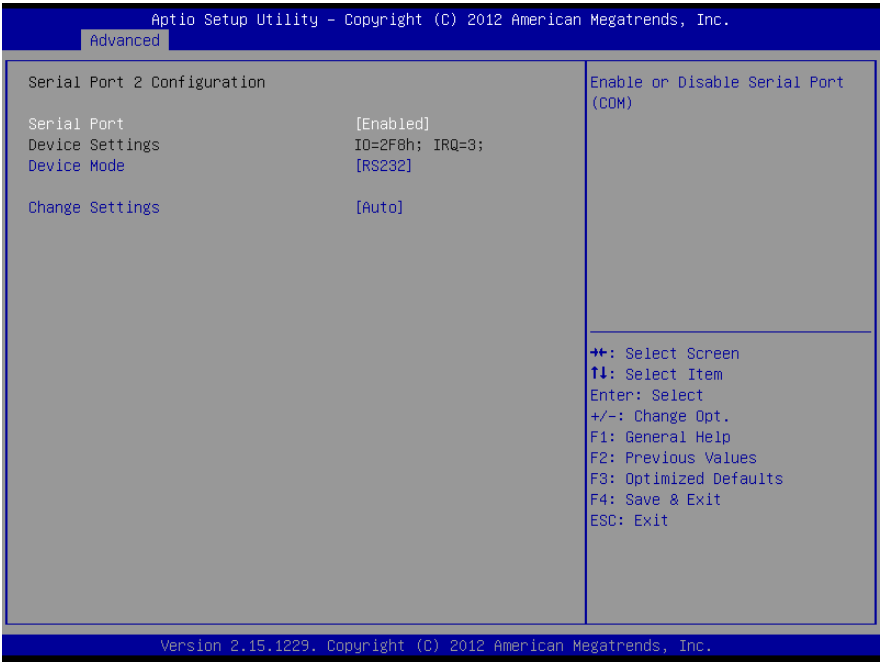
3.4.10.1 Super IO Configuration: Serial Port 1 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Change Settings	Auto	Default
	IO=3F8h; IRQ=4;	
	IO=3F8h; IRQ=3,4;	
	IO=2F8h; IRQ=3,4;	
	IO=3E8h; IRQ=3.4	
	IO=2E8h; IRQ=3,4;	
Allows BIOS to Select Serial Port resource.		

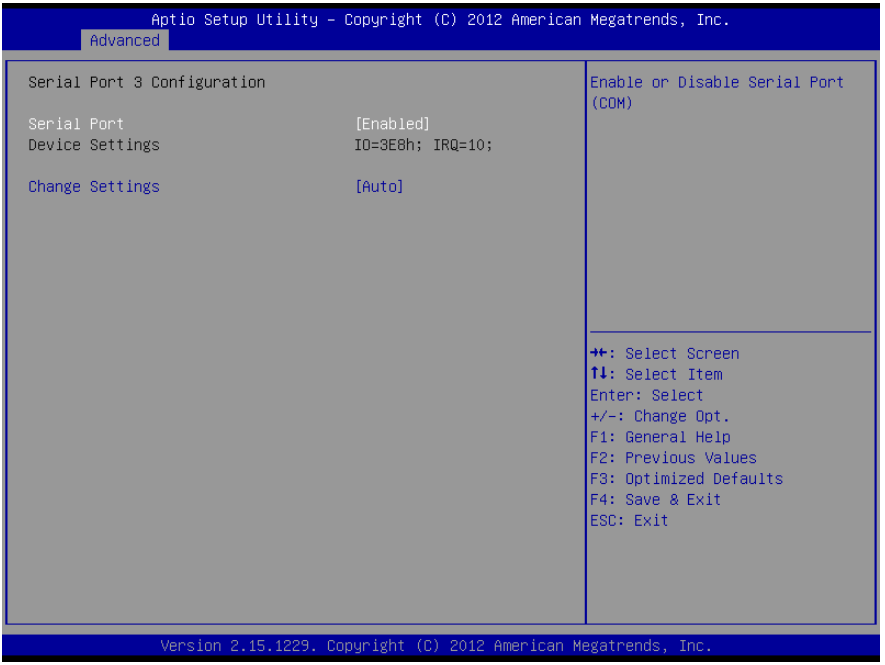
3.4.10.2 Super IO Configuration: Serial Port 2 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings	Auto	Default
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=3,4;	
	IO=2F8h; IRQ=3,4;	
	IO=3E8h; IRQ=3,4;	
	IO=2E8h; IRQ=3,4;	
Allows BIOS to Select Serial Port resource.		

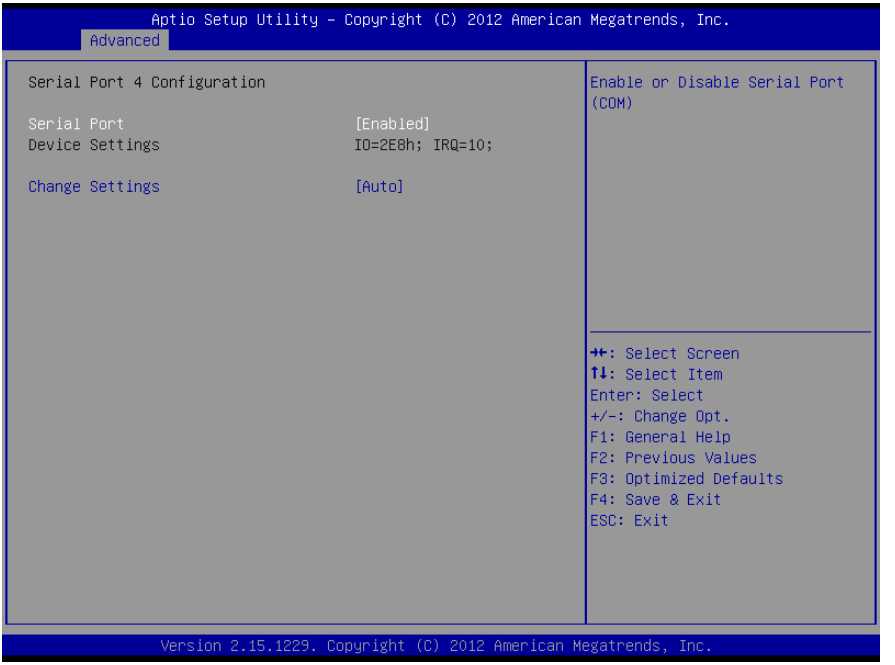
3.4.10.3 Super IO Configuration: Serial Port 3 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Change Settings	Auto	Default
	IO=3E8h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

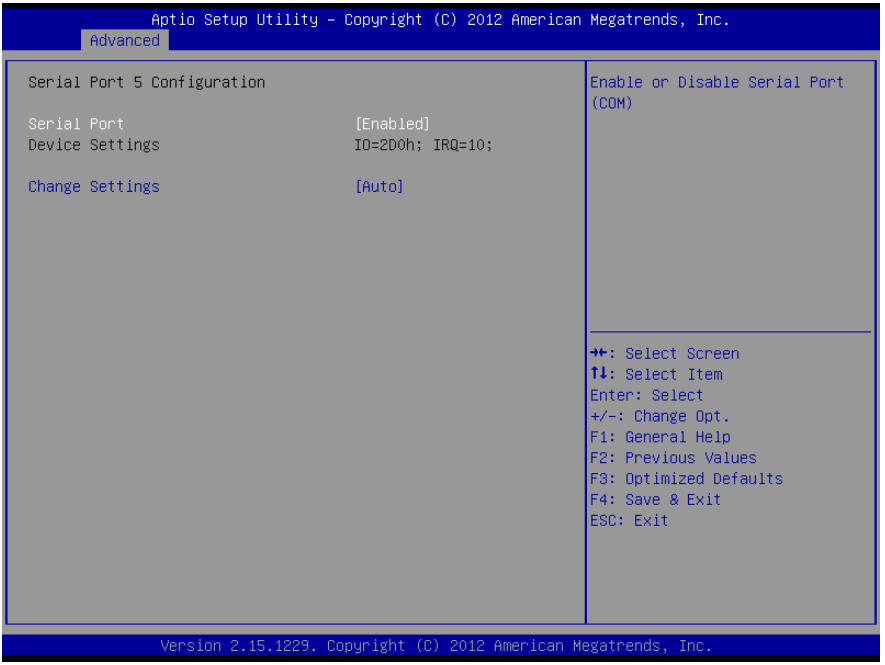
3.4.10.4 Super IO Configuration: Serial Port 4 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Change Settings	Auto	Default
	IO=2E8h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

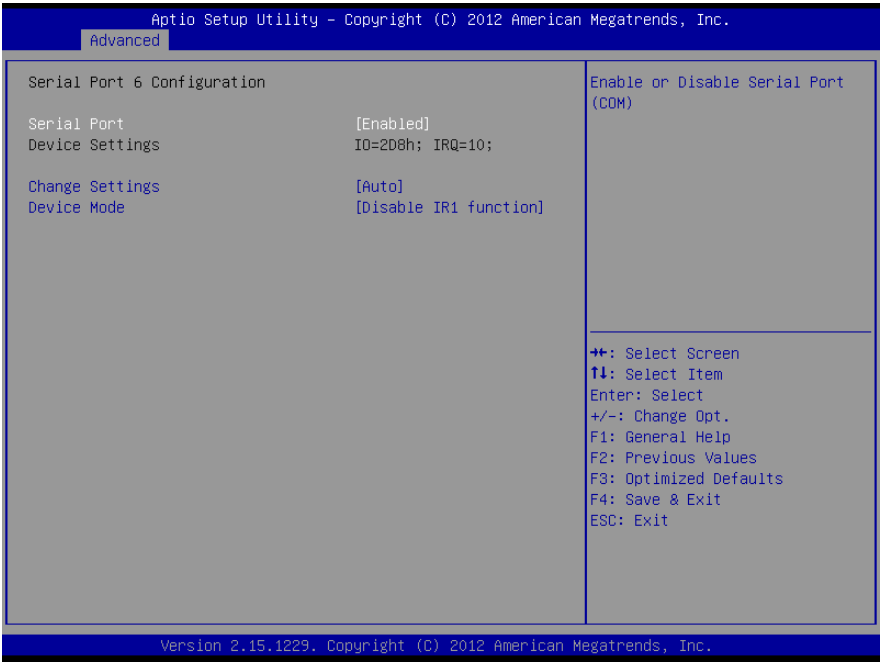
3.4.10.5 Super IO Configuration: Serial Port 5 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings	Auto	Default
	IO=2D0h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

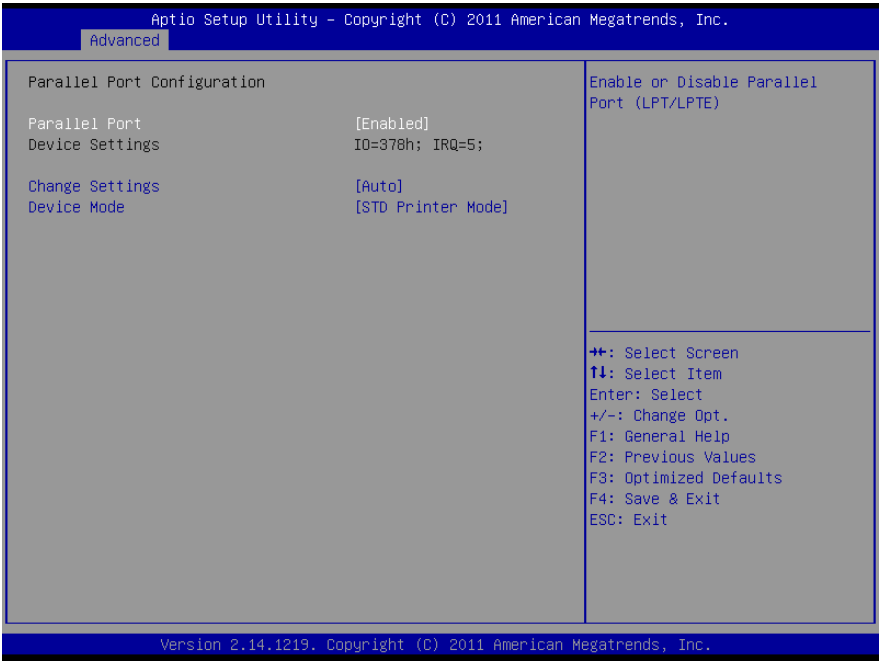
3.4.10.6 Super IO Configuration: Serial Port 6 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings	Auto	Default
	IO=2D8h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

3.4.10.7 Super IO Configuration: Parallel Port Configuration

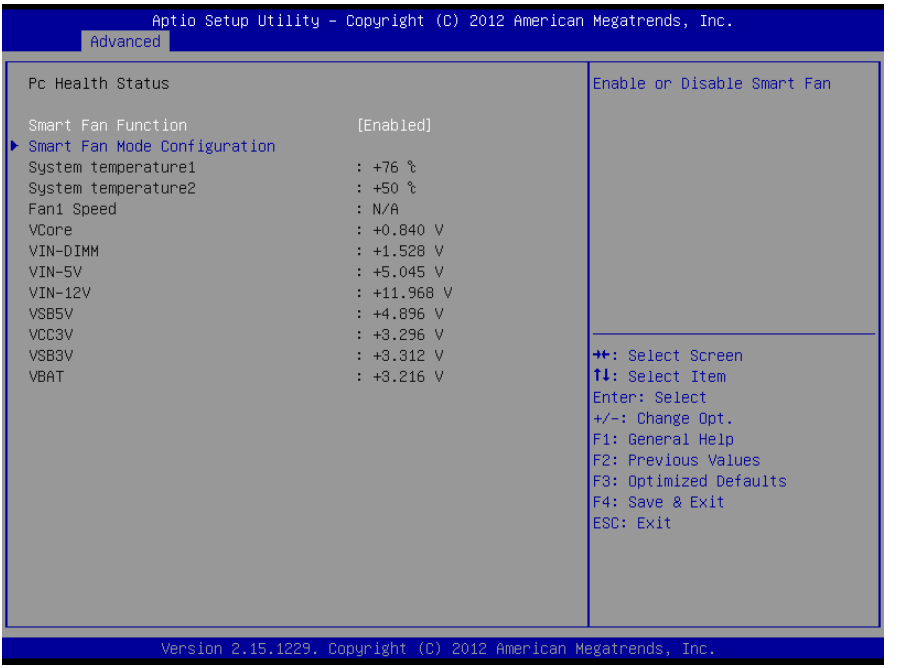


Options summary:

Parallel Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable Parallel port.		
Change Settings (Parallel Port)	Auto	Default
	IO=378h; IRQ=5;	
	IO=378h; IRQ=5,7;	
	IO=278h; IRQ=5,7;	
	IO=3BCh; IRQ=5,7;	
Allows BIOS to Select Serial Port resource.		
Device Mode	STD Printer Mode	Default
	SPP Mode	
	EPP-1.9 and SPP Mode	
	EPP-1.9 and SPP Mode	
	ECP Mode	
	ECP and EPP 1.9 Mode	
	ECP and EPP 1.7 Mode	

Change the Printer Port mode.

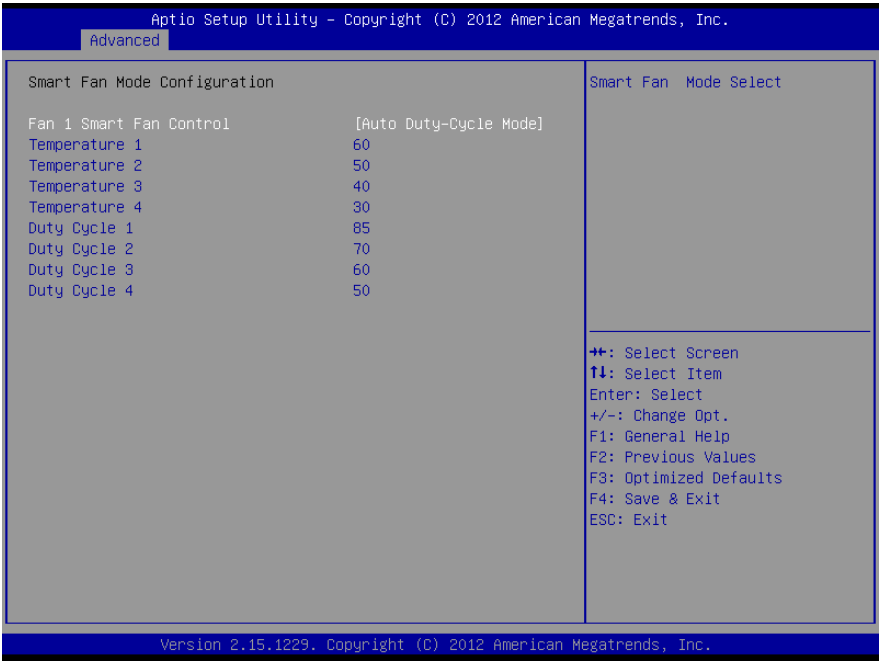
3.4.11 Advanced: F81866 H/W Monitor



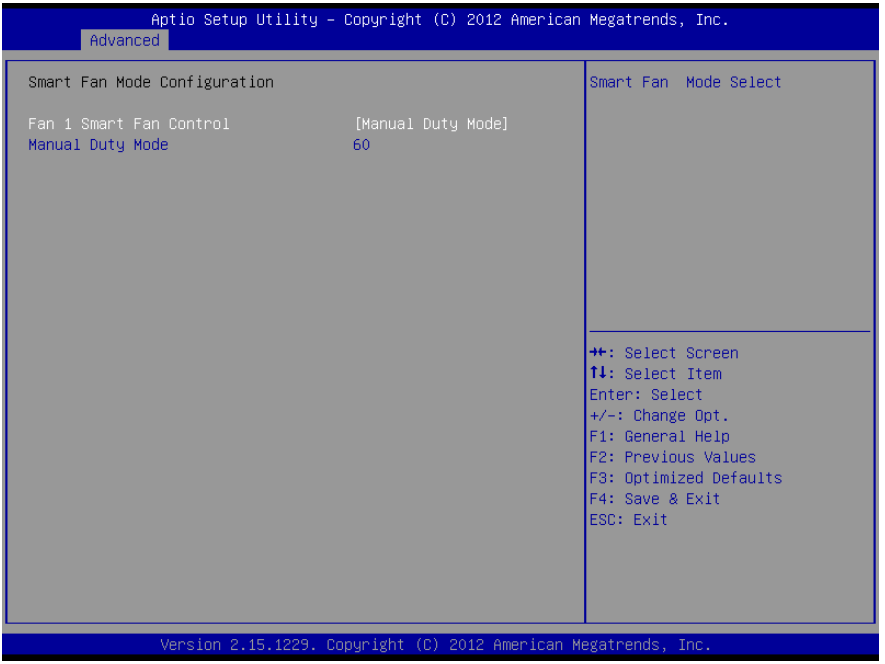
Options summary:

Smart Fan Function	Disabled	
	Enabled	Default
Enable or Disable Smart Fan.		

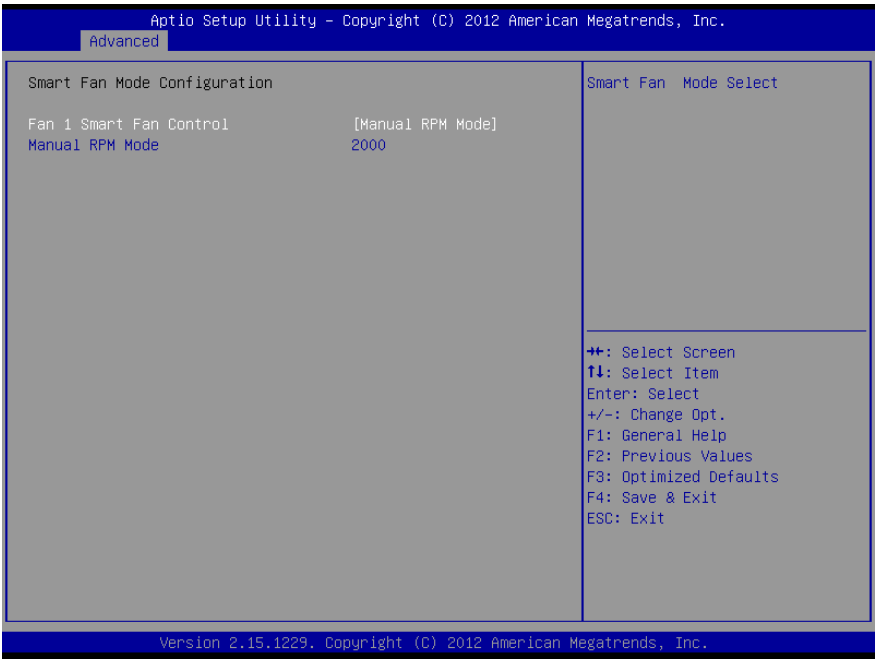
3.4.11.1 F81866 H/W Monitor: Smart Fan Mode Configuration (Auto Duty-Cycle Mode)



3.4.11.2 F81866 H/W Monitor: Smart Fan Mode Configuration (Manual duty Mode)



3.4.11.3 F81866 H/W Monitor: Smart Fan Mode Configuration (Manual RPM Mode)

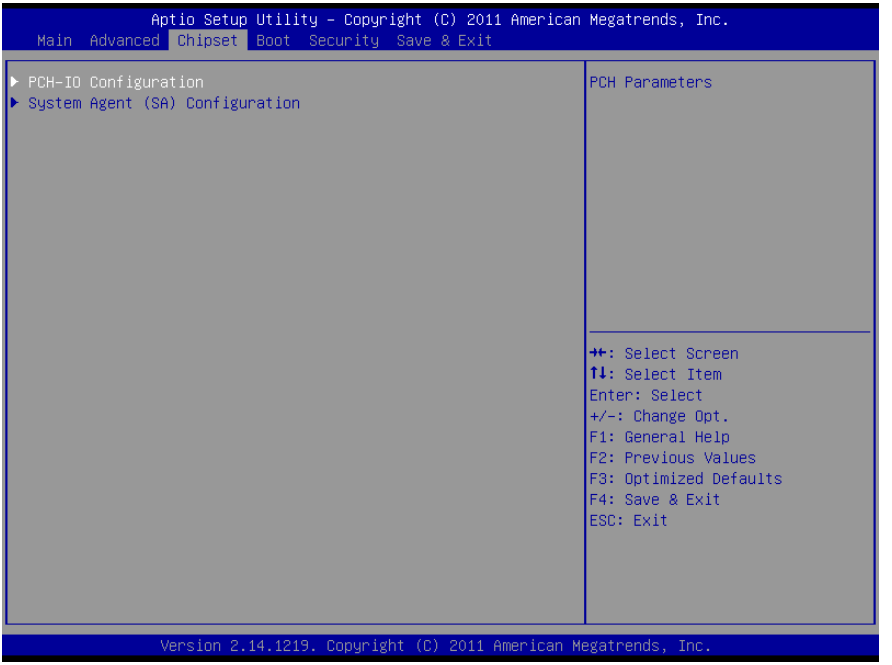


Options summary:

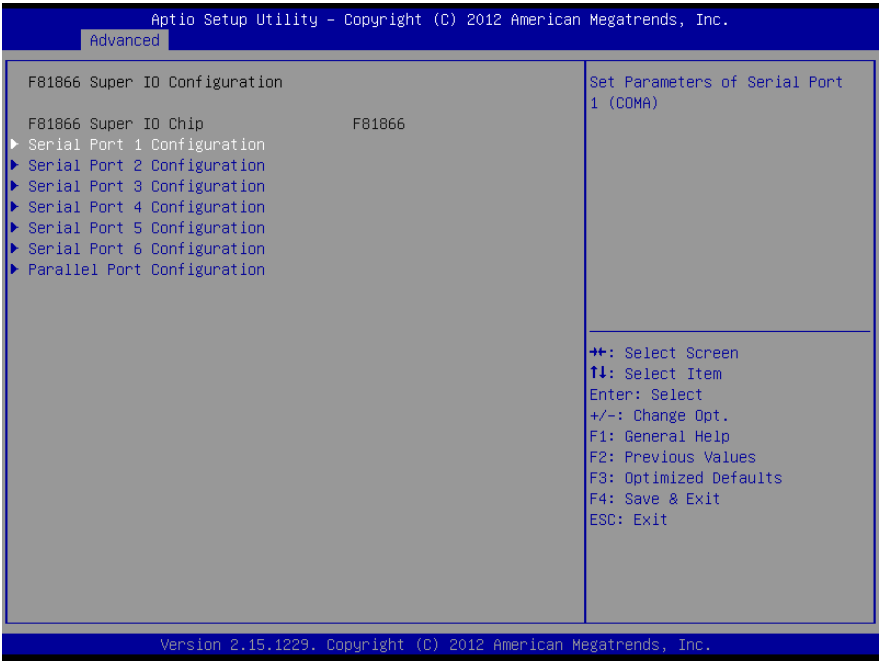
Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	Default
Smart Fan Mode Select		
Temperature 1	60	Default
Temperature 2	50	Default
Temperature 3	40	Default
Temperature 4	30	Default
Duty Cycle 1	85	Default
Duty Cycle 2	70	Default
Duty Cycle 3	60	Default
Duty Cycle 4	50	Default
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100.		

Manual RPM Mode	2000	Default
Manual mode fan control, user can write expected RPM count 500-10000		
Manual Duty Mode	60	Default
Manual mode fan control, user can write expected duty cycle (PWM fan type)1-100		

3.5 Setup submenu: Chipset



3.5.1 Chipset: PCH-IO Configuration

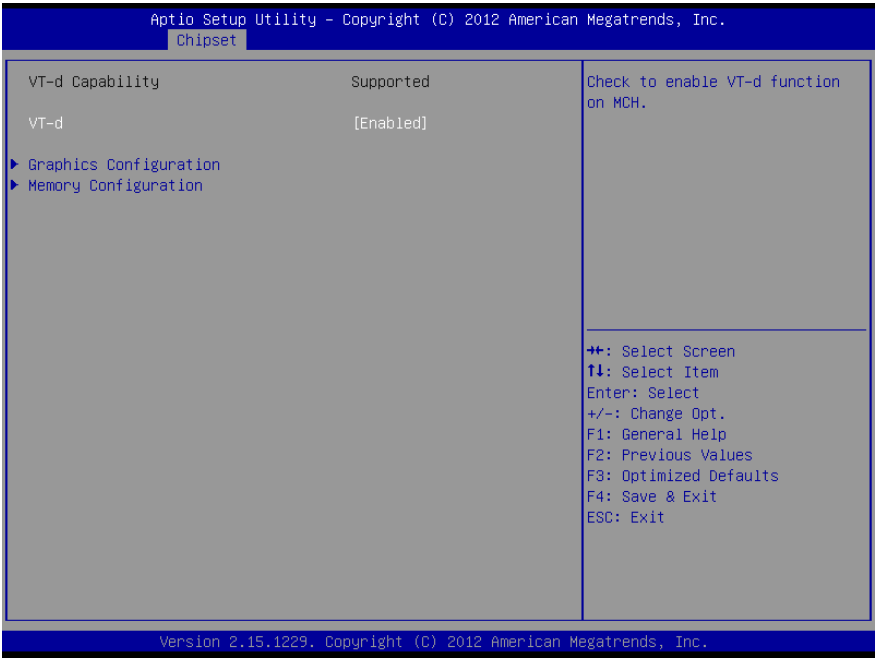


Options summary:

Mini Card2 Controller	Disabled	
	Enabled	Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Default
	Gen1	
	Gen2	
Select PCI Express port speed.		
Mini Card1 Controller	Disabled	
	Enabled	Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Default
	Gen1	
	Gen2	
Select PCI Express port speed.		
PCH LAN Controller	Disabled	
	Enabled	Default

Control the PCI Express Root Port.		
I82583V LAN Controller	Disabled	
	Enabled	Default
Control the PCI Express Root Port		
Azalia	Disabled	
	Enabled	
	Auto	Default
Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled; Enabled = Azalia will be unconditionally enabled; Auto = Azalia will be enabled if present, disabled otherwise.		
Azalia Internal HDMI Codec	Disabled	
	Enabled	Default
Enable or disable internal HDMI codec for Azalia.		
Power Mode	ATX Type	Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Always OFF	
	Always ON	
	Last State	Default
Select AC power state when power is re-applied after a power failure.		
Resume On Ring	Disabled	
	Enabled	Default
Enable/Disable Resume from RI# signal.		

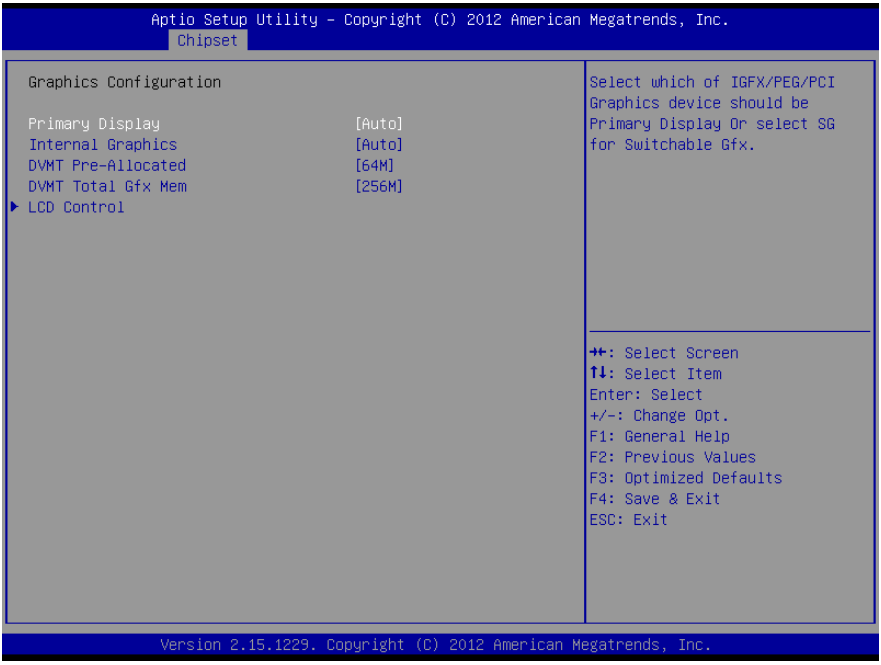
3.5.2 Chipset: System Agent (SA) Configuration



Options summary:

VT-d	Disabled	
	Enabled	Default
Check to enable VT-d function on MCH		

3.5.2.1 System Agent (SA) Configuration: Graphics Configuration

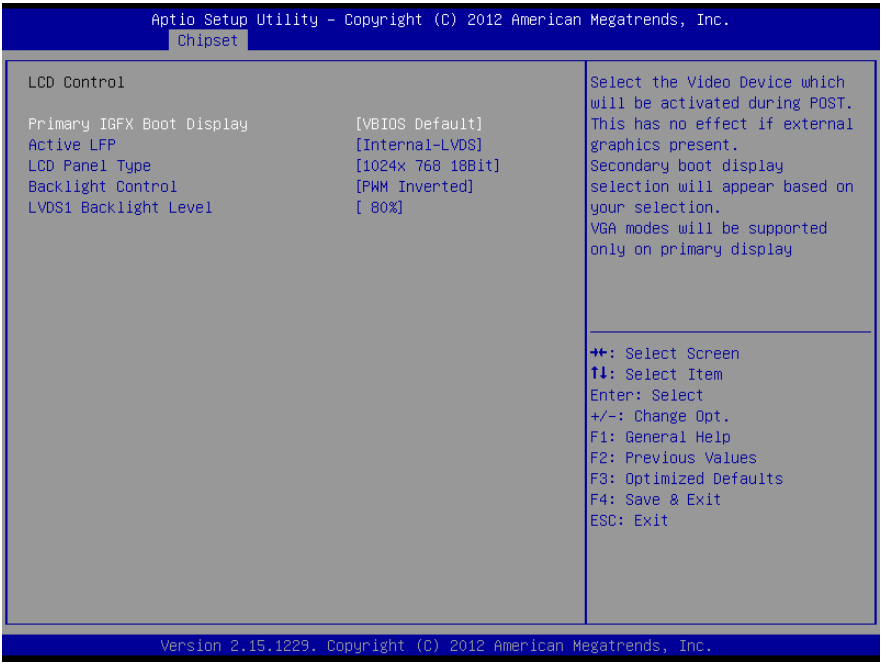


Options summary:

Primary Display	Auto	Default
	IGFX	
	PEG	
	PCI	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.		
Internal Graphics	Auto	Default
	Disabled	
	Enabled	
Keep IGD enabled based on setup options.		
DVMT Pre-Allocated	32MB	
	64MB	Default
	96MB	
	128MB	
	160MB	
	192MB	

	224MB	
	256MB	
	288MB	
	320MB	
	352MB	
	384MB	
	416MB	
	448MB	
	480MB	
	512MB	
	1024MB	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Mem	128MB	Default
	256MB	
	MAX	
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.		

3.5.2.2 Graphics Configuration: LCD Control



Options summary:

Primary Display	VBIOS Default	Default
	CRT	
	DVI	
	LVDS	
	HDMI	
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear base on your selection. VGA modes will be supported only on primary display.		
Active LFP	No LVDS	Default
	Internal –LVDS	
	External -LVDS	
Select the active LFP Configuration. No LVDS: VBIOS does not enable LVDS. Internal-LVDS:VBIOS enables LVDS driver by Integrated encoder. External-LVDS:LFP Driven by PTN-3460		

Internal-LVDS

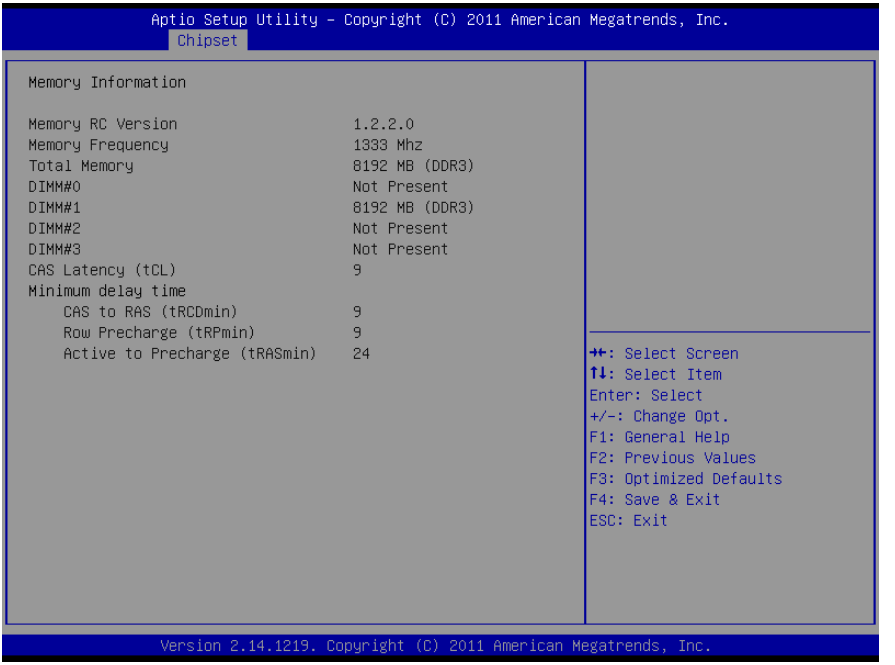
LCD Panel Type	640x 480 18Bit	
	800x 480 18Bit	
	800x 600 18Bit	
	1024x 768 18Bit	Default
	1024x 768 24Bit	
	1280x 768 24Bit	
	1280x102414Bit	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		

External-LVDS

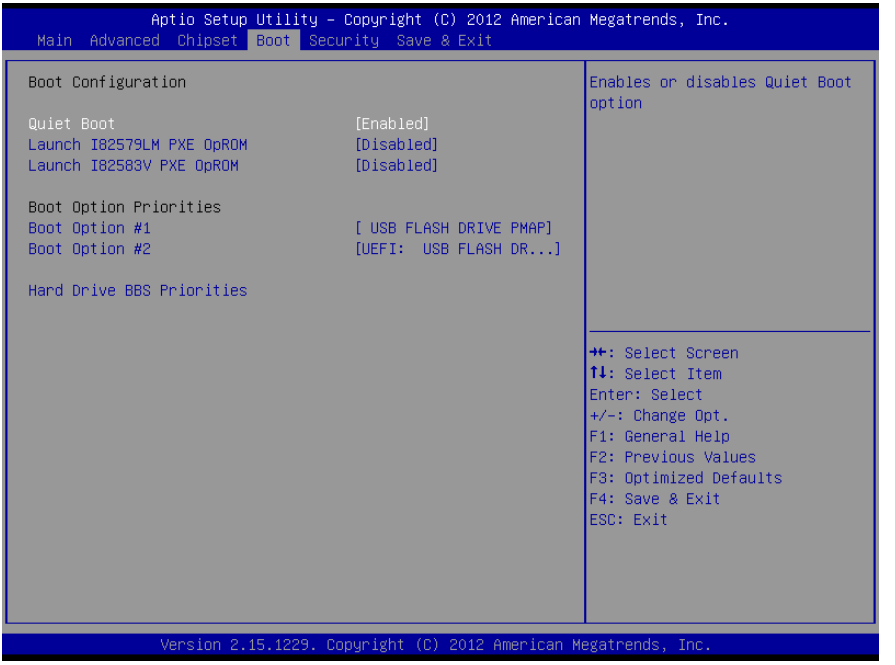
LCD Panel Type	1600x1200 48Bit (Ext. Only)	Default
	1920x1080 48Bit (Ext. Only)	
	1920x1200 48Bit (Ext. Only)	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
Backlight Control	PWM Inverted	Default
	PWM Normal	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		

LVDS1 Backlight Level	100%	
	90%	
	80%	
	70%	Default
	60%	
	50%	
	40%	
	30%	
	20%	
	10%	
	0%	
Select Backlight brightness of LVDS		

3.5.2.3 Chipset: Memory Information



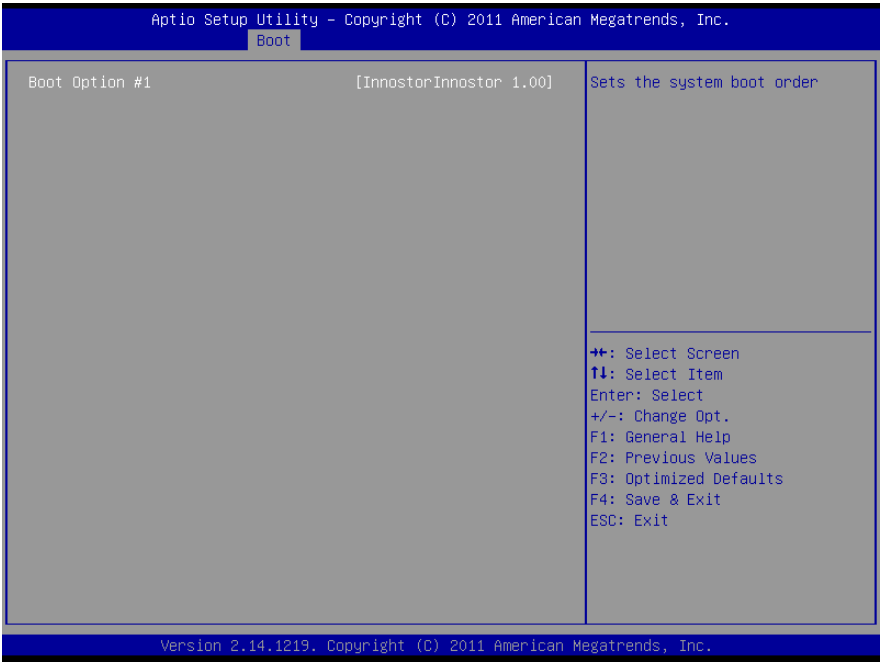
3.6 Setup submenu: Boot



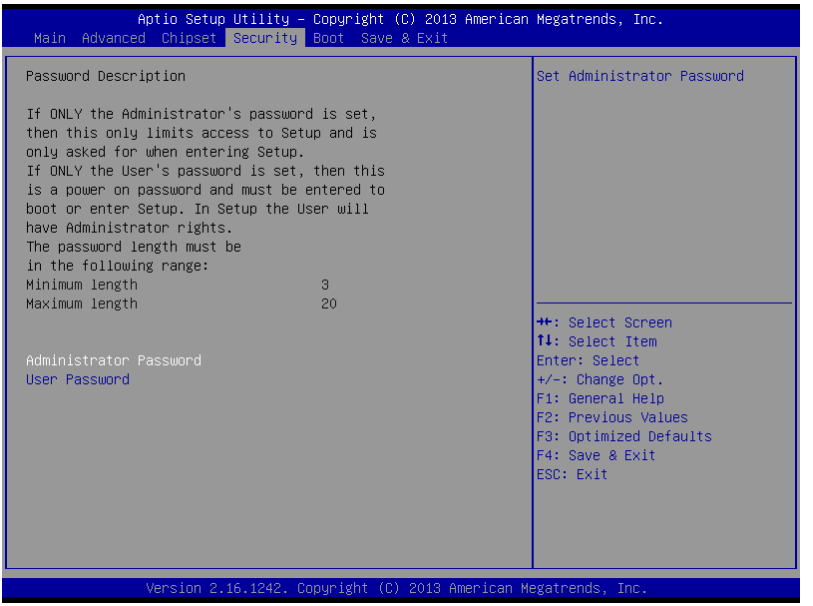
Options summary:

Quiet Boot	Disabled	Default
	Enabled	
En/Disable showing boot logo.		
Launch I82579LM PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option for I82579LM.		
Launch I82583V PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option for I82583V.		

3.6.1 Boot: BBS Priorities



3.7 Setup submenu: Security



Change User/Administrator Password

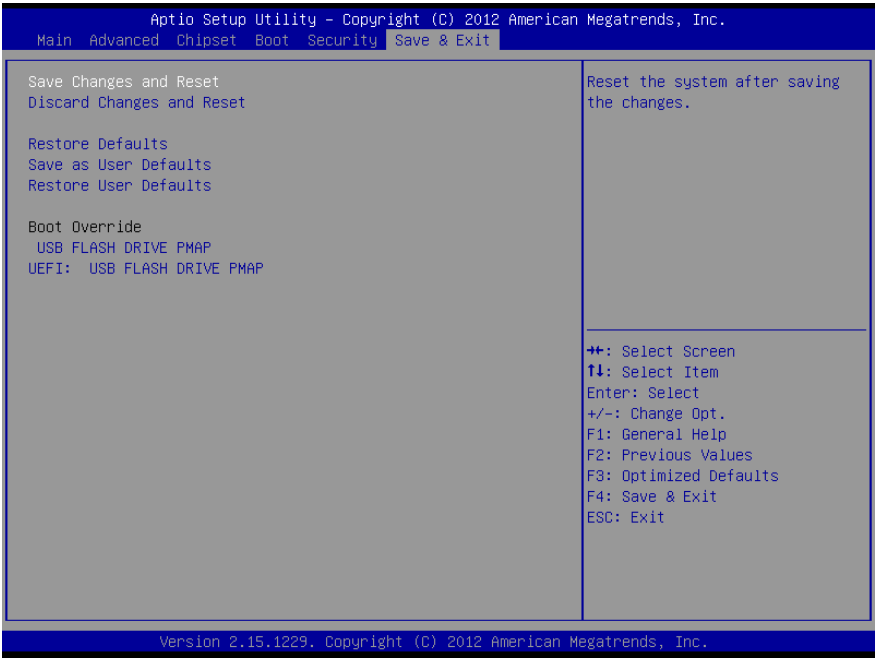
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The EPIC-QM77 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 – Chipset** folder followed by **infinst_autol.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **STEP2 - VGA** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Note 1:

- This motherboard supports VGA and LVDS display devices. In Single Display mode. By default, press **<Ctrl>+<Alt>+<F1>** to switch to VGA device and press **<Ctrl>+<Alt>+<F3>** to switch to LVDS device.
- Before removing the current display device, connect the display device that you want to use, and then press the hot keys to switch to that device.

Note 2: If you are using Windows® XP, you have to install the driver of dotNet Framework first (**dotnetfx35.exe** in **dotNet Framwork** folder).

Step 3 – Install LAN Driver

1. Open the **STEP3 – LAN (Intel_82579)** folder and select your OS

2. Open the .**exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 – Audio** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install ME Drivers

1. Open the **STEP5 – ME SW** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install RAID & AHCI Drivers

Please refer to Appendix E RAID & AHCI Settings

Step 7 – Install TPM Driver

1. Open the **STEP7 – TPM** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 8 – Install Touch Driver

1. Open the **STEP8 – Touch** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions

4. Drivers will be installed automatically

Step 9 – Install USB 3.0 Driver

1. Open the **STEP9 – USB 3.0** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : Super I/O relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
********************************************************************************
```

```
*******************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*******************************************************************************
```

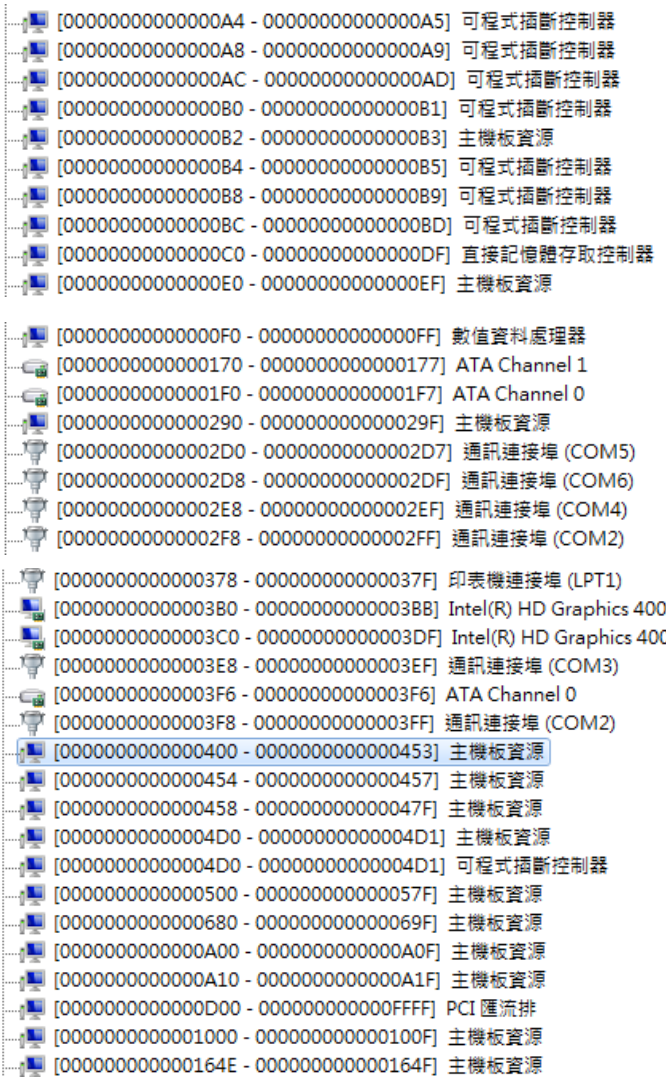
```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
       // WDT output mode setting, level / pulse
       SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*******************************************************************************
```

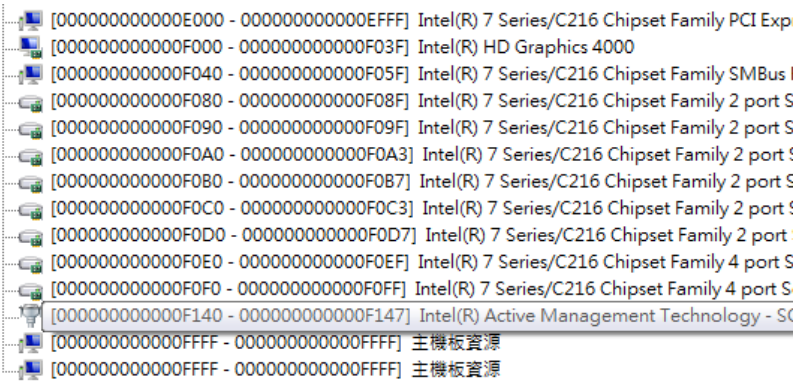
```
*******************************************************************************
VOID    SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID    SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*******************************************************************************
```

Appendix B

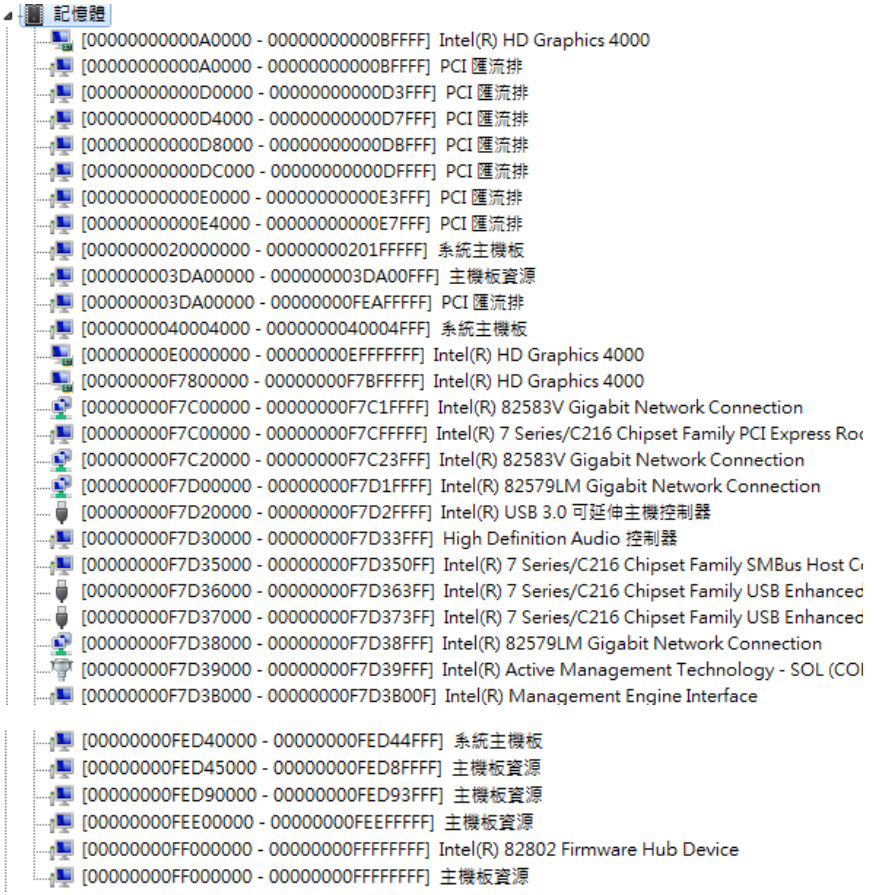
I/O Information

B.1 I/O Address Map

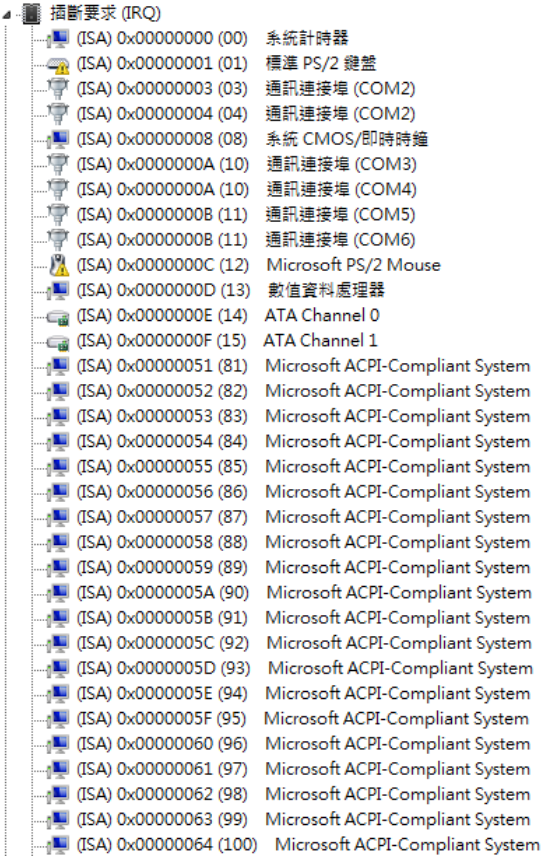

[00000000000000A4 - 00000000000000A5] 可程式插斷控制器
[00000000000000A8 - 00000000000000A9] 可程式插斷控制器
[00000000000000AC - 00000000000000AD] 可程式插斷控制器
[00000000000000B0 - 00000000000000B1] 可程式插斷控制器
[00000000000000B2 - 00000000000000B3] 主機板資源
[00000000000000B4 - 00000000000000B5] 可程式插斷控制器
[00000000000000B8 - 00000000000000B9] 可程式插斷控制器
[00000000000000BC - 00000000000000BD] 可程式插斷控制器
[00000000000000C0 - 00000000000000DF] 直接記憶體存取控制器
[00000000000000E0 - 00000000000000EF] 主機板資源
[00000000000000F0 - 00000000000000FF] 數值資料處理器
[0000000000000170 - 0000000000000177] ATA Channel 1
[00000000000001F0 - 00000000000001F7] ATA Channel 0
[0000000000000290 - 000000000000029F] 主機板資源
[00000000000002D0 - 00000000000002D7] 通訊連接埠 (COM5)
[00000000000002D8 - 00000000000002DF] 通訊連接埠 (COM6)
[00000000000002E8 - 00000000000002EF] 通訊連接埠 (COM4)
[00000000000002F8 - 00000000000002FF] 通訊連接埠 (COM2)
[0000000000000378 - 000000000000037F] 印表機連接埠 (LPT1)
[00000000000003B0 - 00000000000003BB] Intel(R) HD Graphics 4000
[00000000000003C0 - 00000000000003DF] Intel(R) HD Graphics 4000
[00000000000003E8 - 00000000000003EF] 通訊連接埠 (COM3)
[00000000000003F6 - 00000000000003F6] ATA Channel 0
[00000000000003F8 - 00000000000003FF] 通訊連接埠 (COM2)
[0000000000000400 - 0000000000000453] 主機板資源
[0000000000000454 - 0000000000000457] 主機板資源
[0000000000000458 - 000000000000047F] 主機板資源
[00000000000004D0 - 00000000000004D1] 主機板資源
[00000000000004D0 - 00000000000004D1] 可程式插斷控制器
[0000000000000500 - 000000000000057F] 主機板資源
[0000000000000680 - 000000000000069F] 主機板資源
[0000000000000A00 - 0000000000000A0F] 主機板資源
[0000000000000A10 - 0000000000000A1F] 主機板資源
[0000000000000D00 - 000000000000FFFF] PCI 匯流排
[0000000000001000 - 000000000000100F] 主機板資源
[000000000000164E - 000000000000164F] 主機板資源

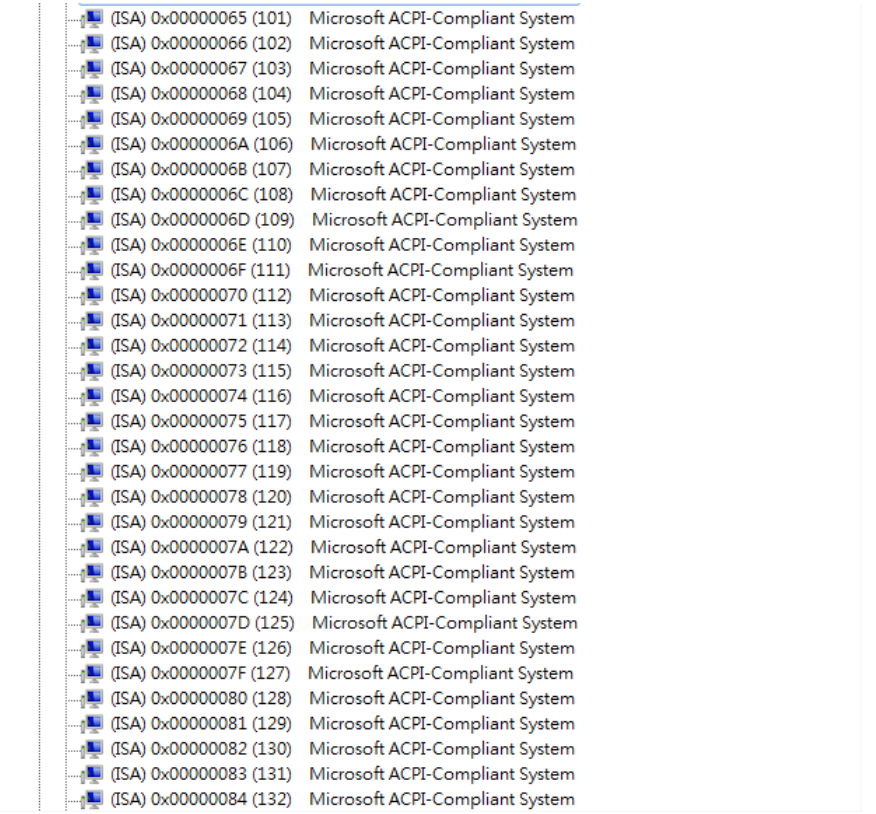

[0000000000000E000 - 0000000000000EFFF] Intel(R) 7 Series/C216 Chipset Family PCI Exp
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics 4000
[000000000000F040 - 000000000000F05F] Intel(R) 7 Series/C216 Chipset Family SMBus
[000000000000F080 - 000000000000F08F] Intel(R) 7 Series/C216 Chipset Family 2 port S
[000000000000F090 - 000000000000F09F] Intel(R) 7 Series/C216 Chipset Family 2 port S
[000000000000F0A0 - 000000000000F0A3] Intel(R) 7 Series/C216 Chipset Family 2 port
[000000000000F0B0 - 000000000000F0B7] Intel(R) 7 Series/C216 Chipset Family 2 port S
[000000000000F0C0 - 000000000000F0C3] Intel(R) 7 Series/C216 Chipset Family 2 port
[000000000000F0D0 - 000000000000F0D7] Intel(R) 7 Series/C216 Chipset Family 2 port
[000000000000F0E0 - 000000000000F0EF] Intel(R) 7 Series/C216 Chipset Family 4 port S
[000000000000F0F0 - 000000000000F0FF] Intel(R) 7 Series/C216 Chipset Family 4 port S
[000000000000F140 - 000000000000F147] Intel(R) Active Management Technology - S
[000000000000FFFF - 000000000000FFFF] 主機板資源
[000000000000FFFF - 000000000000FFFF] 主機板資源

B.2 Memory Address Map



B.3 IRQ Mapping Chart




(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
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(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
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(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
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(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
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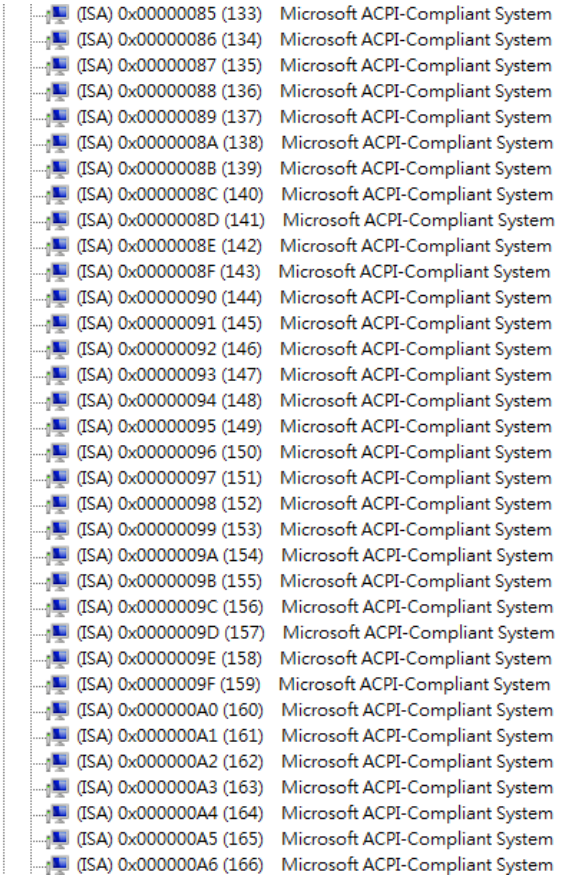
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(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
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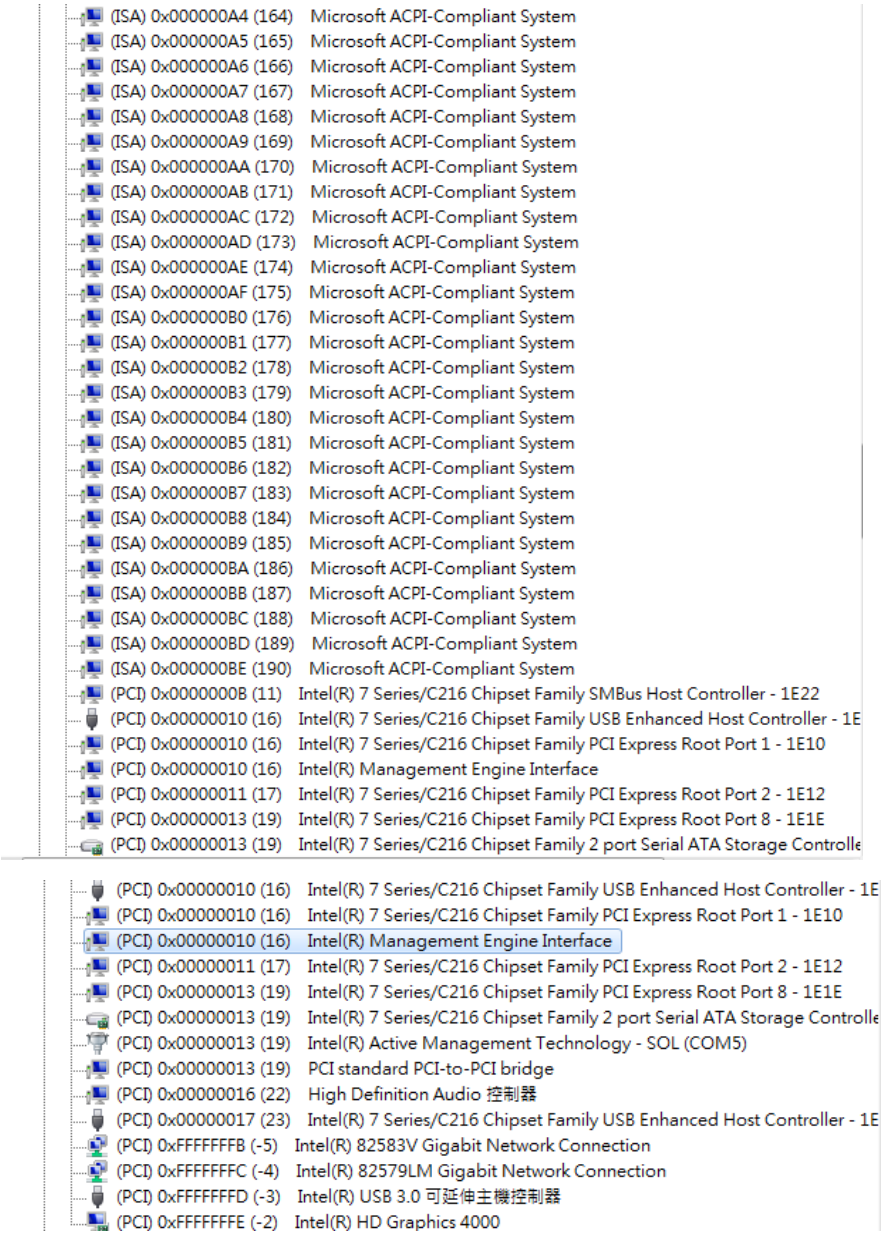
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System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(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
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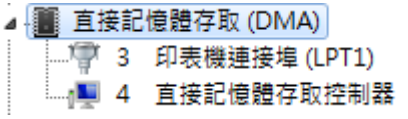
(ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
(ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
(ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
(ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
(ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
(ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
(ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
(ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
(ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
(ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
(ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
(ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
(ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
(PCI) 0x0000000B (11) Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
(PCI) 0x00000010 (16) Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E
(PCI) 0x00000010 (16) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 1 - 1E10
(PCI) 0x00000010 (16) Intel(R) Management Engine Interface
(PCI) 0x00000011 (17) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 2 - 1E12
(PCI) 0x00000013 (19) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 8 - 1E1E
(PCI) 0x00000013 (19) Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controlle

(PCI) 0x00000010 (16) Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E
(PCI) 0x00000010 (16) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 1 - 1E10
(PCI) 0x00000010 (16) Intel(R) Management Engine Interface
(PCI) 0x00000011 (17) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 2 - 1E12
(PCI) 0x00000013 (19) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 8 - 1E1E
(PCI) 0x00000013 (19) Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controlle
(PCI) 0x00000013 (19) Intel(R) Active Management Technology - SOL (COM5)
(PCI) 0x00000013 (19) PCI standard PCI-to-PCI bridge
(PCI) 0x00000016 (22) High Definition Audio 控制器
(PCI) 0x00000017 (23) Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E
(PCI) 0xFFFFFFFB (-5) Intel(R) 82583V Gigabit Network Connection
(PCI) 0xFFFFFFFC (-4) Intel(R) 82579LM Gigabit Network Connection
(PCI) 0xFFFFFFFD (-3) Intel(R) USB 3.0 可延伸主機控制器
(PCI) 0xFFFFFFFE (-2) Intel(R) HD Graphics 4000

B.4 DMA Channel Assignments



Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN2	Touch Screen Connector	PINREX	710-75-09W001		
CN3	SATA Power Connector	PINREX	721-75-02W001		1702150155
CN5	1st Backlight Connector	CATCH	H732-05		
CN6	2nd Backlight Connector	CATCH	H732-05		
CN9	LPT_DIO Connector	Astron	25-2103-213-1G-R		
CN10	Audio Connector	PINREX	712-75-10W001		1709100254
CN13	Front Panel Connector	PINREX	712-75-10W001		
CN14	Amp R-channel Connector	PINREX	712-75-02W001		
CN16	LPC Connector	CATCH	H746-12		1701260200
CN17	Amp L-channel Connector	PINREX	712-75-02W001		
CN18	3G SIM Connector	ACES	50375-00511-001		
USB3	USB2.0 Connector	PINREX	712-75-05W001		1700050207
USB4	USB2.0 Connector	PINREX	712-75-05W001		1700050207
USB5	USB2.0 Connector	PINREX	712-75-05W001		1700050207
USB6	USB2.0 Connector	PINREX	712-75-05W001		1700050207
COM3	COM3 RS-232 Serial	PINREX	712-75-09W001		1701090150

	Port Connector				
COM4	COM4 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
COM5	COM5 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
COM6	COM6 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
KB1	PS/2 Keyboard Mouse Connector	CATCH	H752-06		1700060155
FAN1	Fan Connector	PINREX	742-75-04W001		
BAT1	RTC Battery Connector	CATCH	2P 1201-700-02S		
LVDS1	1st LVDS Connector	E-call	0109-02-522-300		
LVDS2	2nd LVDS Connector	E-call	0109-02-522-300		

Appendix D

Electrical Specifications for I/O Ports

D.1 Electrical Specifications for I/O Ports

I/O	Reference	Signal Name	Rate Output
LVDS Port 1	LVDS1	VCC	+3.3V/1A or +5V/1A
LVDS Port 2	LVDS2	VCC	+3.3V/1A or +5V/1A
LPC Port	CN16	+3.3V	+3.3V/0.5A
LVDS Port 1 Inverter / Backlight Connector	CN5	VDD	+5V/2A or +12V/2A
LVDS Port 2 Inverter / Backlight Connector	CN6	VDD	+5V/2A or +12V/2A
+5V Output for SATA HDD	CN3	+5V	+5V/1A
Audio I/O Port	CN10	+5V	+5V/0.5A
2Pin PWRIN (Optional)	CN15	+12V	+12V/3A
ATX 4Pin PWRIN	CN12	+12V	+12V/6A
FAN	FAN1	+5V	+5V/0.5A
Mini Card Slot	CN8	+3.3VSB +1.5V	+3.3V/1A +1.5V/0.375A
mSATA Slot	CN7	+3.3VSB +1.5V	+3.3V/1A +1.5V/0.375A

USB 3.0 Ports 1 and 2	USB1	+5VSB	+5V/1A (per channel)
USB 2.0 Ports 3.4.5.6	USB3/USB4 USB5/USB6	+5VSB	+5V/0.5A (per channel)
COM Port 2	COM1B	+5V/+12V	+5V/1A or +12V/1A
Digital IO Port	CN9	GPIO0~GPIO15	+5V (Ext. Pull Up)
VGA / DVI Ports	CN1	VGA: +5V DVI : +5V	+5V/0.5A

D.2 DIO Programming

EPIC-QM77 utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode
(2) Modify the data of configuration registers
(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

D.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x82(Note4)	0(Note5)		PE
DIO-2 Pin Status	0x06(Note6)	0x82(Note7)	1(Note8)		BUSY
DIO-3 Pin Status	0x06(Note9)	0x82(Note10)	2(Note11)		ACK#
DIO-4 Pin Status	0x06(Note12)	0x82(Note13)	3(Note14)		SLIN#
DIO-5 Pin Status	0x06(Note15)	0x82(Note16)	4(Note17)		PINIT#
DIO-6 Pin Status	0x06(Note18)	0x82(Note19)	5(Note20)		ERR#
DIO-7 Pin Status	0x06(Note21)	0x82(Note22)	6(Note23)		AFD#
DIO-8 Pin Status	0x06(Note24)	0x82(Note25)	7(Note26)		STB#
DIO-11 Pin Status	0x06(Note3-1)	0x8A(Note4-1)	0(Note5-1)		PD0
DIO-12 Pin Status	0x06(Note6-1)	0x8A(Note7-1)	1(Note8-1)		PD1
DIO-13 Pin Status	0x06(Note9-1)	0x8A(Note10-1)	2(Note11-1)		PD2
DIO-14 Pin Status	0x06(Note12-1)	0x8A(Note13-1)	3(Note14-1)		PD3
DIO-15 Pin Status	0x06(Note15-1)	0x8A(Note16-1)	4(Note17-1)		PD4
DIO-16 Pin Status	0x06(Note18-1)	0x8A(Note19-1)	5(Note20-1)		PD5

DIO-17 Pin Status	0x06(Note21-1)	0x8A(Note22-1)	6(Note23-1)		PD6
DIO-18 Pin Status	0x06(Note24-1)	0x8A(Note25-1)	7(Note26-1)		PD7

D.4 Digital I/O Sample Program

```
********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN   // This parameter is represented from Note3
#define byte   DInput1Reg   // This parameter is represented from Note4
#define byte   DInput1Bit   // This parameter is represented from Note5
#define byte   DInput2LDN   // This parameter is represented from Note6
#define byte   DInput2Reg   // This parameter is represented from Note7
#define byte   DInput2Bit   // This parameter is represented from Note8
#define byte   DInput3LDN   // This parameter is represented from Note9
#define byte   DInput3Reg   // This parameter is represented from Note10
#define byte   DInput3Bit   // This parameter is represented from Note11
#define byte   DInput4LDN   // This parameter is represented from Note12
#define byte   DInput4Reg   // This parameter is represented from Note13
#define byte   DInput4Bit   // This parameter is represented from Note14
#define byte   DInput5LDN   // This parameter is represented from Note15
#define byte   DInput5Reg   // This parameter is represented from Note16
#define byte   DInput5Bit   // This parameter is represented from Note17
#define byte   DInput6LDN   // This parameter is represented from Note18
#define byte   DInput6Reg   // This parameter is represented from Note19
#define byte   DInput6Bit   // This parameter is represented from Note20
#define byte   DInput7LDN   // This parameter is represented from Note21
#define byte   DInput7Reg   // This parameter is represented from Note22
#define byte   DInput7Bit   // This parameter is represented from Note23
#define byte   DInput8LDN   // This parameter is represented from Note24
#define byte   DInput8Reg   // This parameter is represented from Note25
#define byte   DInput8Bit   // This parameter is represented from Note26
********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
*********************************************************************************
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput11LDN   // This parameter is represented from Note3-1
#define byte   DInput11Reg   // This parameter is represented from Note4-1
#define byte   DInput11Bit   // This parameter is represented from Note5-1
#define byte   DInput12LDN   // This parameter is represented from Note6-1
#define byte   DInput12Reg   // This parameter is represented from Note7-1
#define byte   DInput12Bit   // This parameter is represented from Note8-1
#define byte   DInput13LDN   // This parameter is represented from Note9-1
#define byte   DInput13Reg   // This parameter is represented from Note10-1
#define byte   DInput13Bit   // This parameter is represented from Note11-1
#define byte   DInput14LDN   // This parameter is represented from Note12-1
#define byte   DInput14Reg   // This parameter is represented from Note13-1
#define byte   DInput14Bit   // This parameter is represented from Note14-1
#define byte   DInput15LDN   // This parameter is represented from Note15-1
#define byte   DInput15Reg   // This parameter is represented from Note16-1
#define byte   DInput15Bit   // This parameter is represented from Note17-1
#define byte   DInput16LDN   // This parameter is represented from Note18-1
#define byte   DInput16Reg   // This parameter is represented from Note19-1
#define byte   DInput16Bit   // This parameter is represented from Note20-1
#define byte   DInput17LDN   // This parameter is represented from Note21-1
#define byte   DInput17Reg   // This parameter is represented from Note22-1
#define byte   DInput17Bit   // This parameter is represented from Note23-1
#define byte   DInput18LDN   // This parameter is represented from Note24-1
#define byte   DInput18Reg   // This parameter is represented from Note25-1
#define byte   DInput18Bit   // This parameter is represented from Note26-1
*********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput11LDN   // This parameter is represented from Note27-1
#define byte   DOutput11Reg   // This parameter is represented from Note28-1
#define byte   DOutput11Bit   // This parameter is represented from Note29-1
#define byte   DOutput11Val   // This parameter is represented from Note30-1
#define byte   DOutput12LDN   // This parameter is represented from Note31-1
#define byte   DOutput12Reg   // This parameter is represented from Note32-1
#define byte   DOutput12Bit   // This parameter is represented from Note33-1
#define byte   DOutput12Val   // This parameter is represented from Note34-1
#define byte   DOutput13LDN   // This parameter is represented from Note35-1
#define byte   DOutput13Reg   // This parameter is represented from Note36-1
#define byte   DOutput13Bit   // This parameter is represented from Note37-1
#define byte   DOutput13Val   // This parameter is represented from Note38-1
#define byte   DOutput14LDN   // This parameter is represented from Note39-1
#define byte   DOutput14Reg   // This parameter is represented from Note40-1
#define byte   DOutput14Bit   // This parameter is represented from Note41-1
#define byte   DOutput14Val   // This parameter is represented from Note42-1
#define byte   DOutput15LDN   // This parameter is represented from Note43-1
#define byte   DOutput15Reg   // This parameter is represented from Note44-1
#define byte   DOutput15Bit   // This parameter is represented from Note45-1
#define byte   DOutput15Val   // This parameter is represented from Note46-1
#define byte   DOutput16LDN   // This parameter is represented from Note47-1
#define byte   DOutput16Reg   // This parameter is represented from Note48-1
#define byte   DOutput16Bit   // This parameter is represented from Note49-1
#define byte   DOutput16Val   // This parameter is represented from Note50-1
#define byte   DOutput17LDN   // This parameter is represented from Note51-1
#define byte   DOutput17Reg   // This parameter is represented from Note52-1
#define byte   DOutput17Bit   // This parameter is represented from Note53-1
#define byte   DOutput17Val   // This parameter is represented from Note54-1
#define byte   DOutput18LDN   // This parameter is represented from Note55-1
#define byte   DOutput18Reg   // This parameter is represented from Note56-1
#define byte   DOutput18Bit   // This parameter is represented from Note57-1
#define byte   DOutput18Val   // This parameter is represented from Note58-1
*********************************************************************************
```

```
*****************************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //       Example, Read Digital I/O Pin 3 status
         // Output :
         //      InputStatus :
         //              0: Digital I/O Pin level is low
         //              1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //       Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****************************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*******************************************************************************
VOID    SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID    SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*******************************************************************************
```

```
*****************************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, OutputEnableReg);
         TmpValue = IOReadByte(SIOData);
         TmpValue |= (1 << BitNum);
         IOWriteByte(SIOData, OutputEnableReg);
         SIOExitMBPnPMode();
}
*****************************************************************************************
```

Appendix E

RAID & AHCI Settings

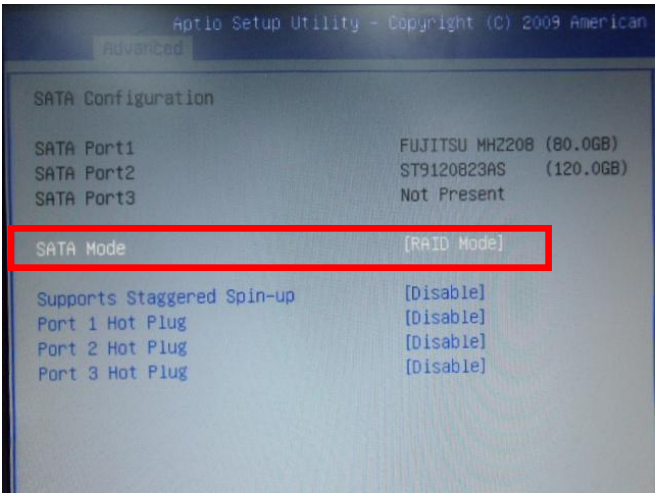
E1 Setting RAID

OS installation to setup RAID Mode

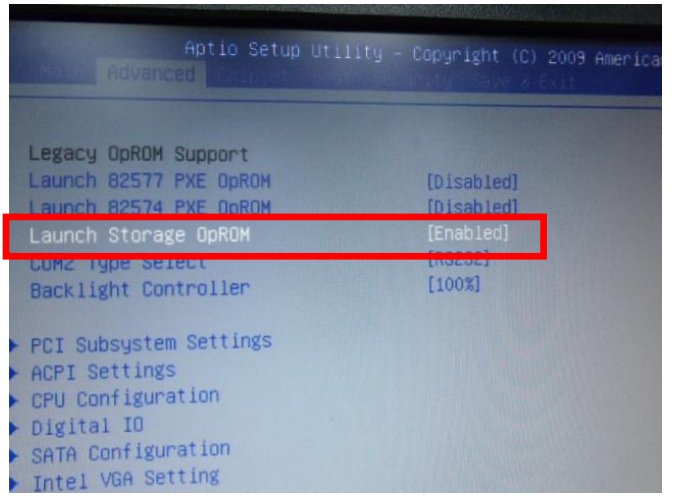
Step 1: Copy the files below from "Driver CD ->Step7- RAID & AHCI" to Disk

Step 2: Connect the USB Floppy (disk with RAID files) to the board

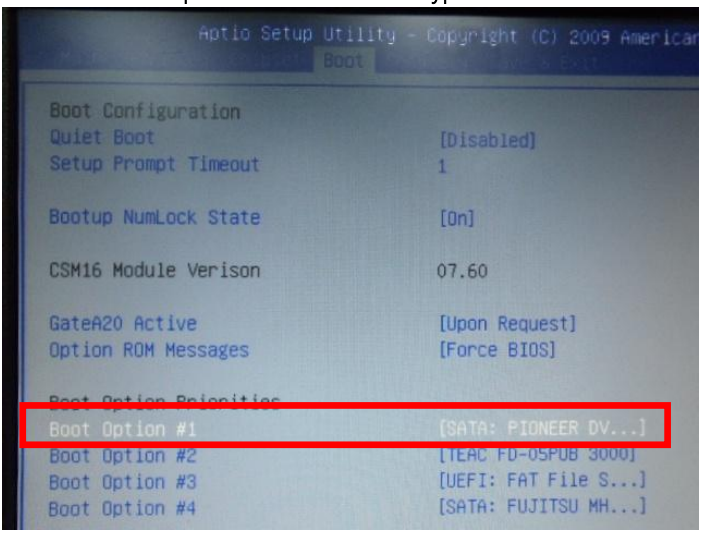
Step 3: The setting procedures " In BIOS Setup Menu"
A: Advanced -> SATA Configuration -> SATA Mode -> RAID Mode



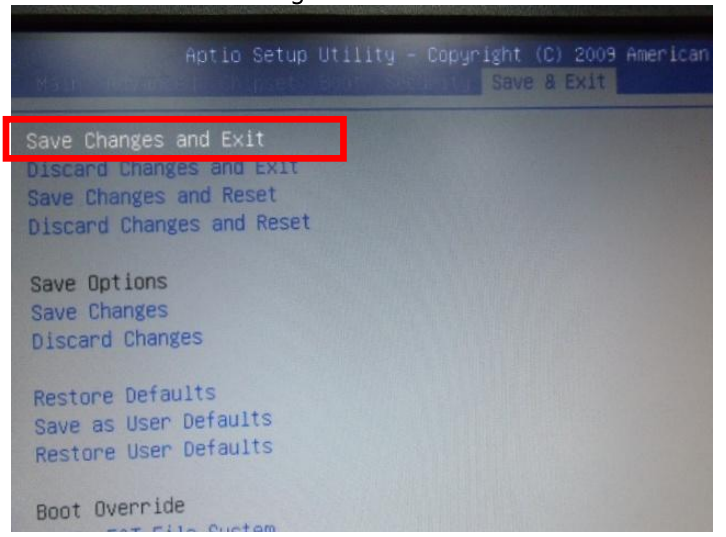
Step 4: The setting procedures "In BIOS Setup Menu"
B: Advanced -> Launch Storage OpROM -> Enabled



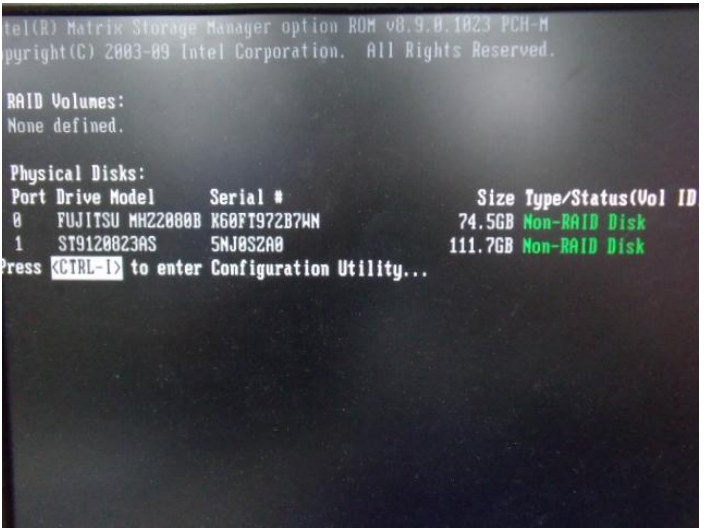
Step 5: The setting procedures "In BIOS Setup Menu"
C: Boot -> Boot Option #1 -> DVD-ROM Type



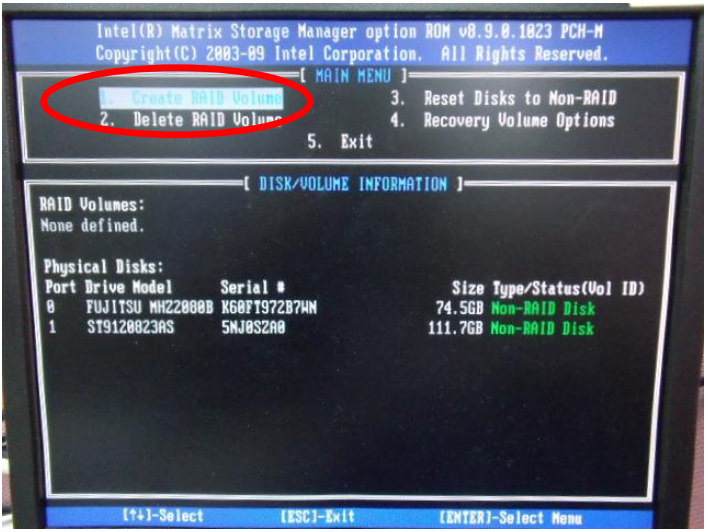
Step 6: The setting procedures "In BIOS Setup Menu"
D: Save & Exit -> Save Changes and Exit



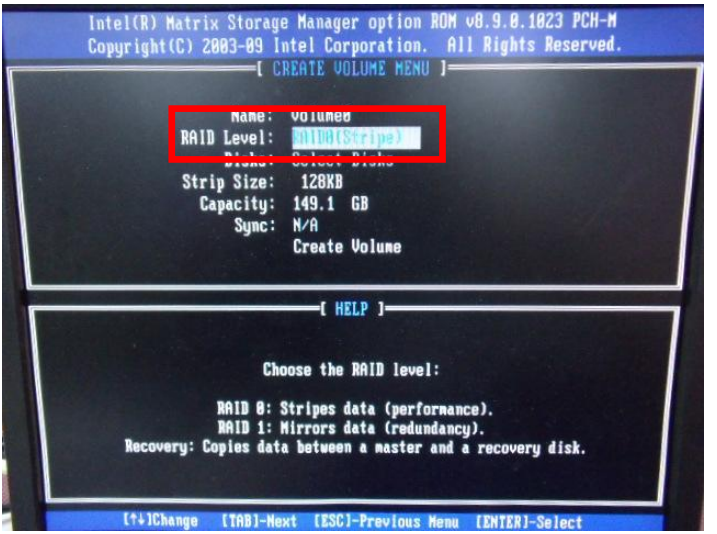
Step 7: Press Ctrl-I to enter MAIN MENU



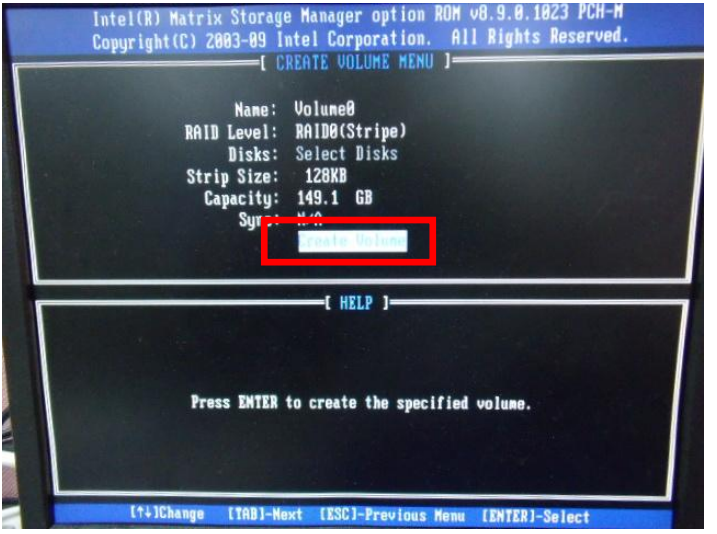
Step 8: Choose "1.Create RAID Volume"



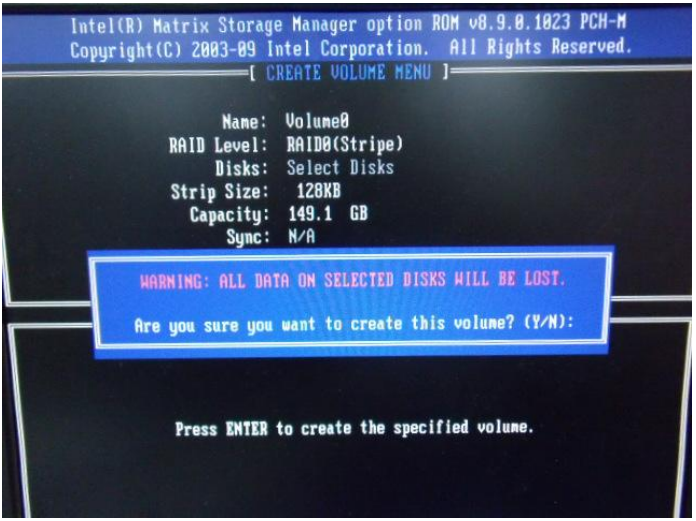
Step 9: RAID Level -> RAID0(Stripe)



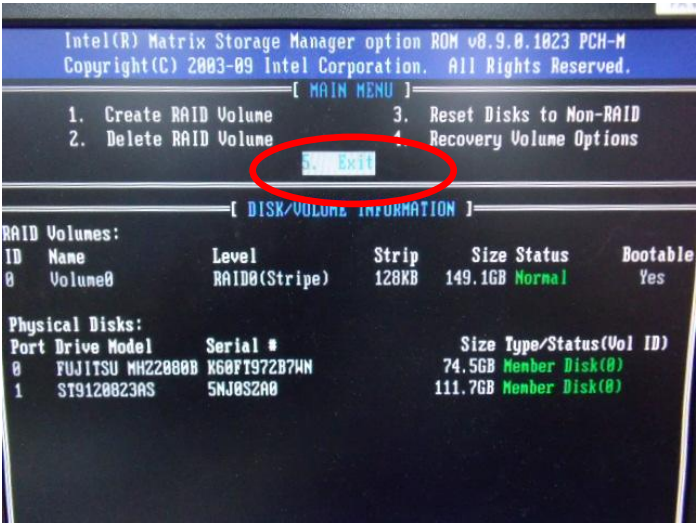
Step 10: Choose "Create Volume"



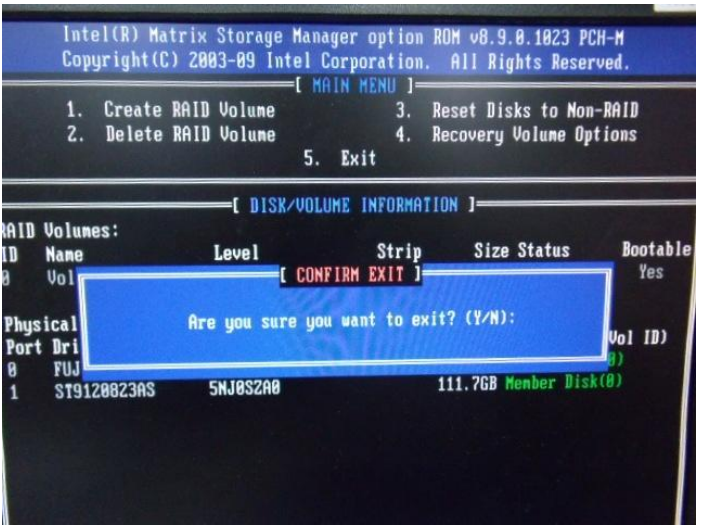
Step 11: Choose "Y"



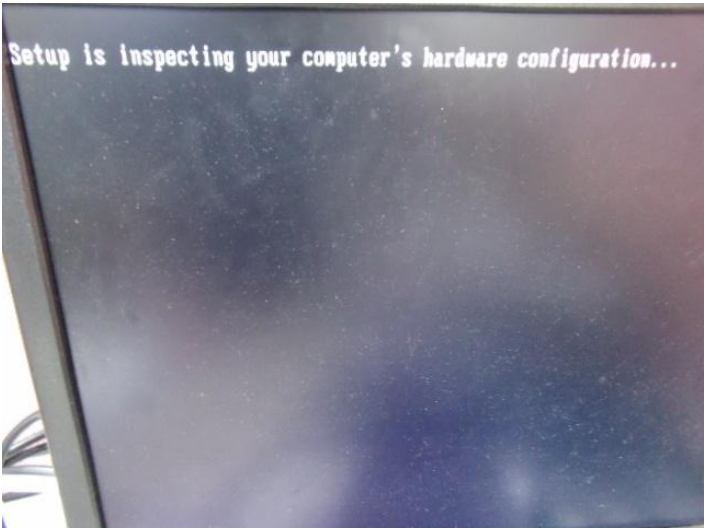
Step 12: Choose "5. Exit"



Step 13: Choose "**Y**"

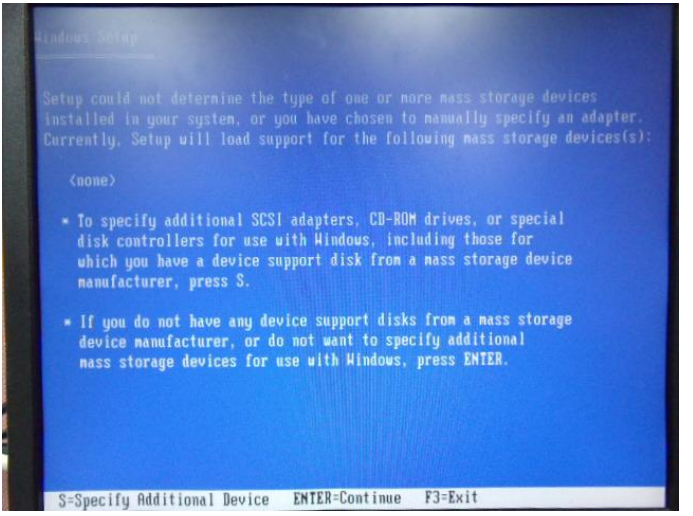


Step 14: Setup OS

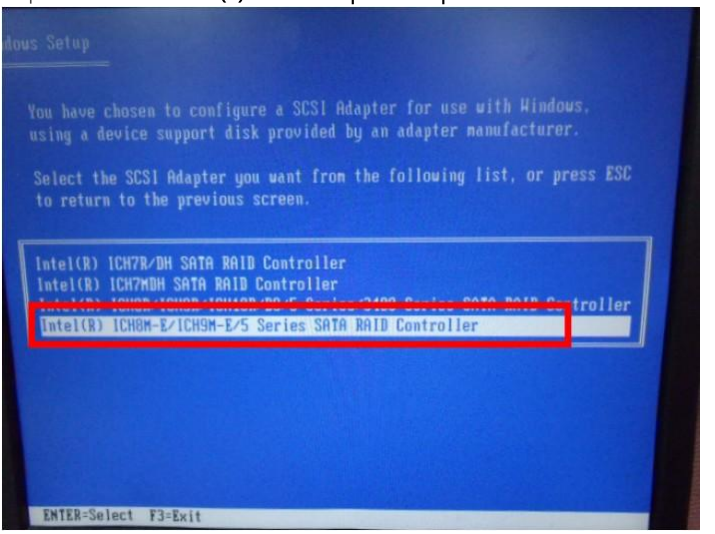


Step 15: Press "**F6**"

Step 16: Choose "**S**"

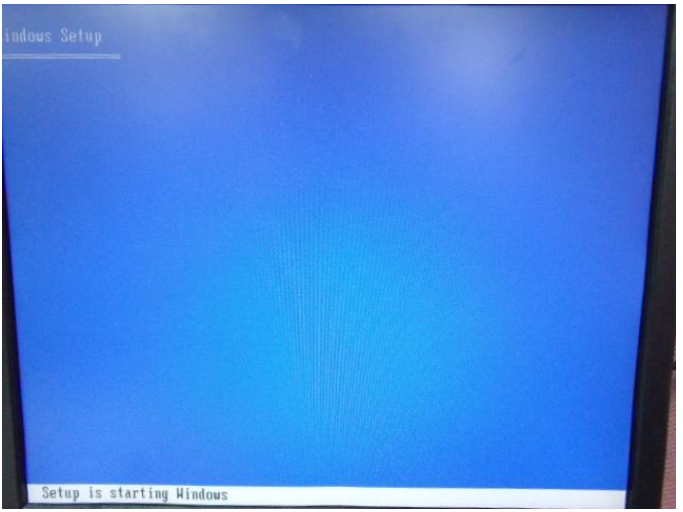


Step 17: Choose "**Intel(R) Mobile Express Chipset SATA RAID Controller**"



Step 18: It will show the model number you select and then press "**ENTER**"

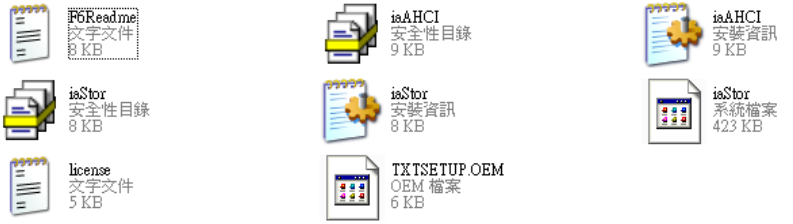
Step 19: Setup is starting Windows



E.2 Setting AHCI

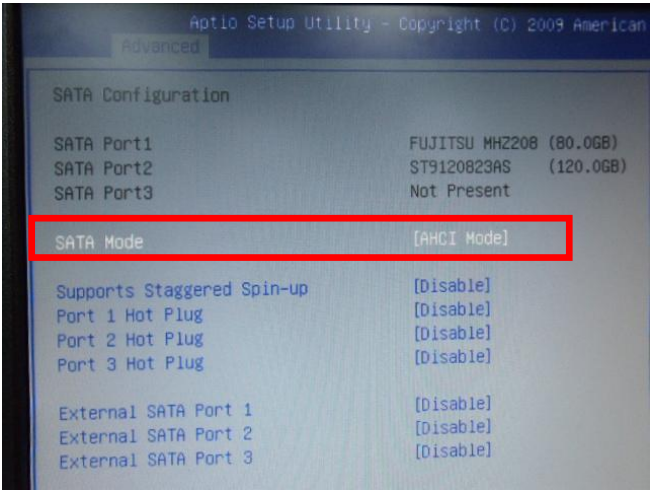
OS installation to setup AHCI Mode

Step 1: Copy the files below from "*Driver CD -> Step7- RAID & AHCI"* to Disk

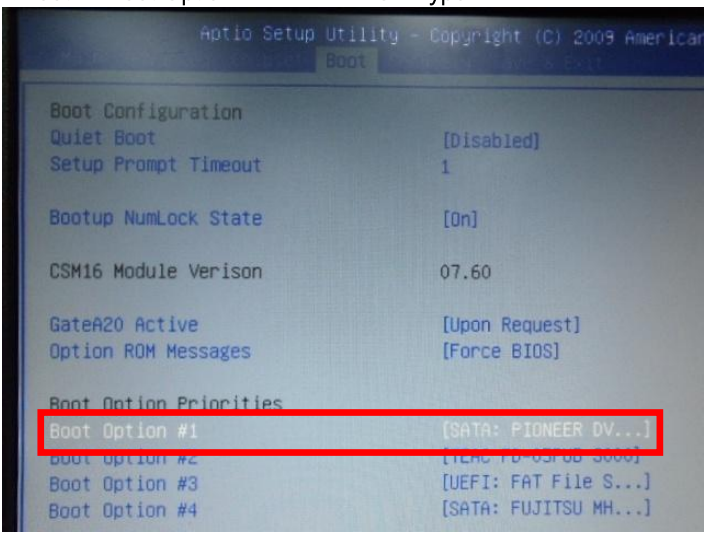


Step 2: Connect the USB Floppy (disk with AHCI files) to the board

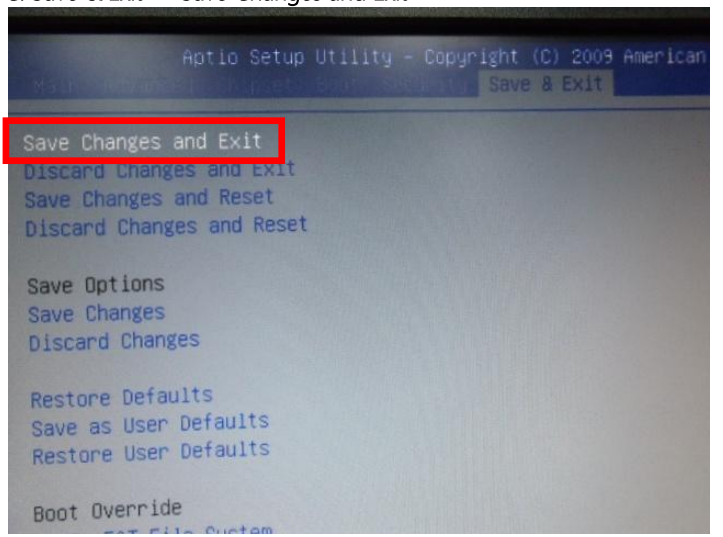
Step 3: The setting procedures " In BIOS Setup Menu"
A: Advanced -> SATA Configuration -> SATA Configuration -> SATA Mode -> AHCI Mode



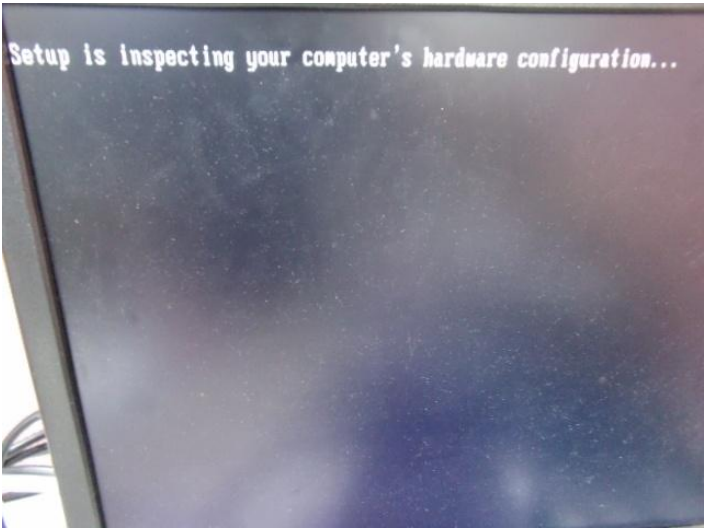
Step 4: The setting procedures "In BIOS Setup Menu"
B: Boot -> Boot Option #1 -> DVD-ROM Type



Step 5: The setting procedures "In BIOS Setup Menu"
C: Save & Exit -> Save Changes and Exit

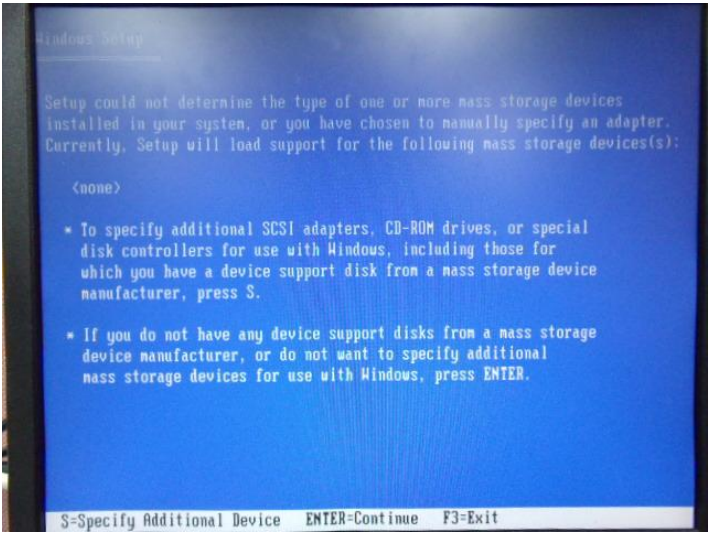


Step 6: Setup OS

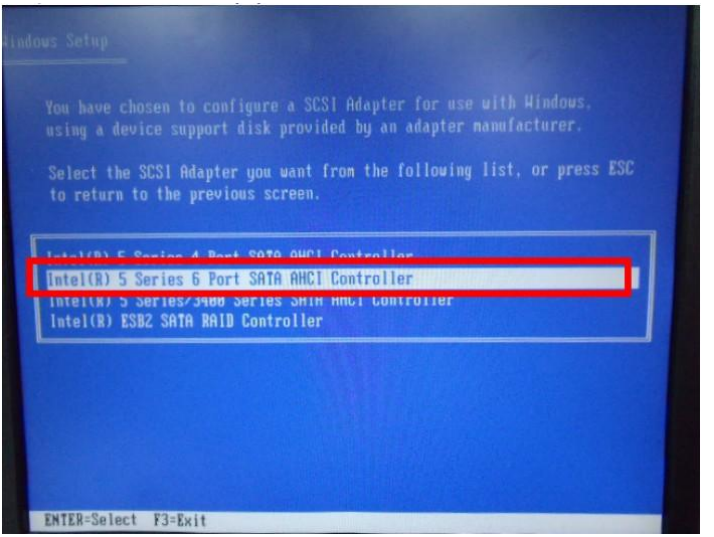


Step 7: Press "F6"

Step 8: Choose "S"



Step 9: Choose "**Intel(R) 7 Series Chipset Family SATA AHCI Controller**"



Step 10: It will show the model number you select and then press "**ENTER**"

Step 11: Setup is loading files